

BME 202 Electronics

Lecture 10: Field Effect Transistors – Part 2





MOSFETs have characteristics similar to those of JFETs and additional characteristics that make then very useful.

There are two types of MOSFETs:

Depletion-Type

Enhancement-Type

The Drain (D) and Source (S) connect to the to *n*-type regions. These *n*-typed regions are connected via an *n*-channel. This *n*-channel is connected to the Gate (G) via a thin insulating layer of silicon dioxide (SiO₂).

The *n*-type material lies on a *p*-type substrate that may have an additional terminal connection called the Substrate (SS).

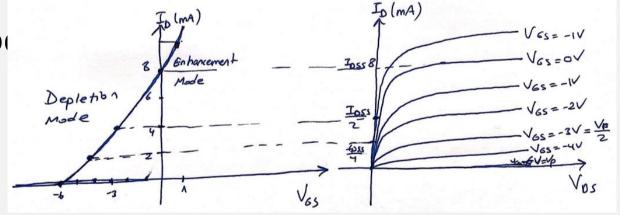
Basic MOSFET Operation



A depletion-type MOSFET can operate in two modes:

Depletion mode

Enhancement mo



Depletion Mode Operation



(D-MOSFET)

The characteristics are similar to a JFET.

when $V_{GS} = 0$ V, $I_D = I_{DSS}$ when $V_{GS} < 0$ V, $I_D < I_{DSS}$

The formula used to plot the transfer curve for a JFET applies to a D-MOSFET as well:

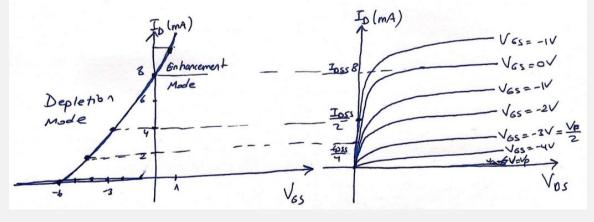
$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

(D-MOSFET)

 $V_{GS} > 0 V, I_D$ increases above I_{DSS} $(I_D > I_{DSS})$

The formula used to plot the transfer curve still applies:

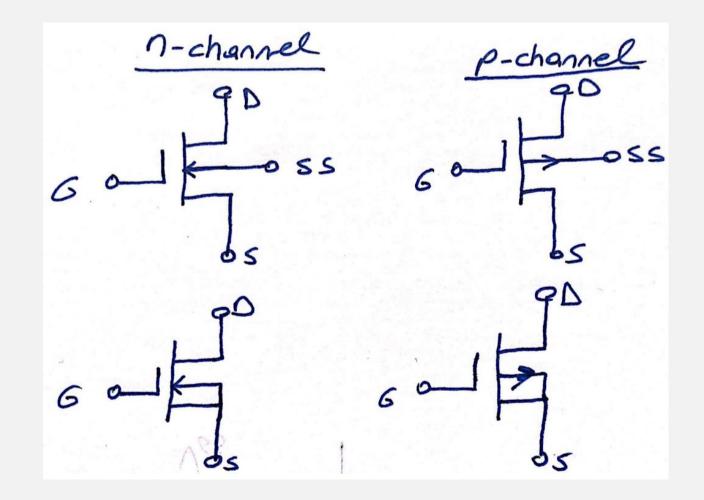
$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$



Note that V_{GS} is now positive





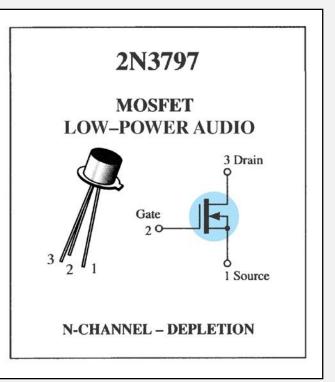




Maximum Ratings

MAXIMUM RATINGS

Rating	Symbol	Value	Unit	
Drain–Source Voltage 2N3797	V _{DS}	20	Vdc	
Gate-Source Voltage	V _{GS}	±10	Vdc	
Drain Current	ID	20	mAdc	
Total Device Dissipation @ $T_A = 25^{\circ}C$ Derate above 25°C	P _D	200 1.14	mW mW/°C	
Junction Temperature Range	Тј	+175	°C	
Storage Channel Temperature Range	T _{stg}	-65 to +200	°C	



Specification Sheet



Electrical Characteristics

Characteristic		Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS						
Drain Source Breakdown Voltage ($V_{GS} = -7.0 V, I_D = 5.0 \mu A$)	2N3797	V _{(BR)DSX}	20	25	-	Vdc
Gate Reverse Current (1) $(V_{GS} = -10 \text{ V}, V_{DS} = 0)$ $(V_{GS} = -10 \text{ V}, V_{DS} = 0, T_A = 150^{\circ}\text{C})$		I _{GSS}	1 1		1.0 200	pAdc
Gate Source Cutoff Voltage ($I_D = 2.0 \ \mu A, V_{DS} = 10 \ V$)	2N3797	V _{GS(off)}	-	-5.0	-7.0	Vdc
Drain-Gate Reverse Current (1) ($V_{DG} = 10 \text{ V}, 1_S = 0$)		l _{DGO}	-	-	1.0	pAdc
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current ($V_{DS} = 10 \text{ V}, V_{GS} = 0$)	2Ņ3797	I _{DSS}	2.0	2.9	6.0	mAdc
On-State Drain Current ($V_{DS} = 10 \text{ V}, V_{GS} = +3.5 \text{ V}$)	2N3797	I _{D(on)}	9.0	14	18	mAde
SMALL-SIGNAL CHARACTERISTICS						
Forward Transfer Admittance $(V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1.0 \text{ kHz})$	2N3797	y _{fs}	1500	2300	3000	μmhos
$(V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz})$	2N3797		1500	-	1	
Output Admittance ($1_{DS} = 10$ V, V $_{GS} = 0$, f = 1.0 kHz)	2N3797	y _{os}	-	27	60	µmhos
Input Capacitance $(V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz})$	2N3797	C _{iss}	-	6.0	8.0	pF
Reverse Transfer Capacitance ($V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$)		C _{rss}	-	0.5	0.8	pF
FUNCTIONAL CHARACTERISTICS						
Noise Figure ($V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1.0 \text{ kHz}, R_S = 3 \text{ megohms}$)		NF	-	3.8	-	dB

E-Type MOSFET Construction



The Drain (D) and Source (S) connect to the to *n*-type regions. These *n*-type regions are connected via an *n*-channel

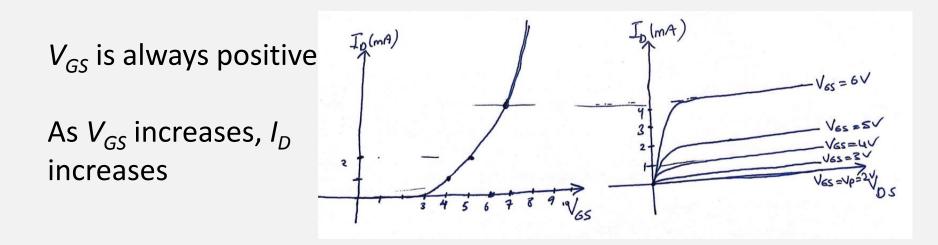
The Gate (G) connects to the p-type substrate via a thin insulating layer of silicon dioxide (SiO₂)

There is no channel

The *n*-type material lies on a *p*-type substrate that may have an additional terminal connection called the Substrate (SS)



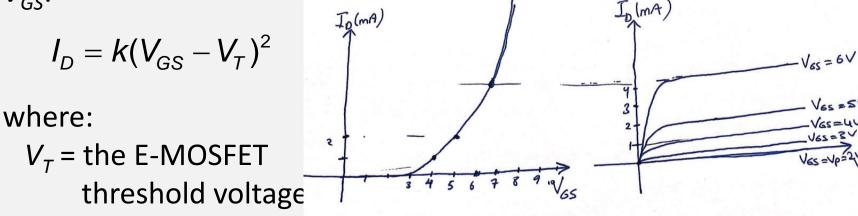
The enhancement-type MOSFET (E-MOSFET) operates only in the enhancement mode.



As V_{GS} is kept constant and V_{DS} is increased, then I_D saturates (I_{DSS}) and the saturation level (V_{DSSat}) is reached



To determine I_D given V_{GS} :



k, a constant, can be determined by using values at a specific point and the formula:

$$k = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2}$$

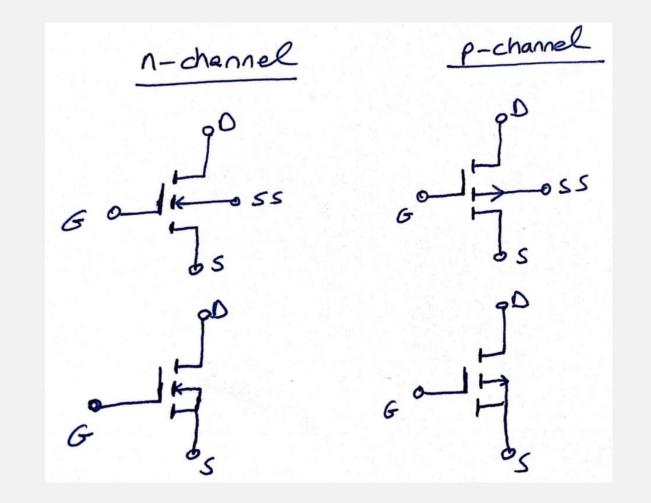
 V_{DSsat} can be calculated using:

$$V_{DSsat} = V_{GS} - V_{T}$$



The *p*-channel enhancement-type MOSFET is similar to its *n*-channel counterpart, except that the voltage polarities and current directions are reversed.





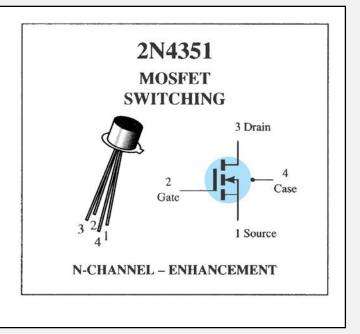


Maximum Ratings

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DS}	25	Vdc
Drain–Gate Voltage	V _{DG}	30	Vdc
Gate-Source Voltage*	V _{GS}	30	Vdc
Drain Current	ID	30	mAdc
Total Device Dissipation @ $T_A = 25^{\circ}C$ Derate above 25°C	P _D	300 1.7	mW mW/°C
Junction Temperature Range	Tj	175	°C
Storage Temperature Range	T _{stg}	-65 to +175	°C

* Transient potentials of ± 75 Volt will not cause gate-oxide failure.



Specification Sheet

Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($I_D = 10 \ \mu$ A, $V_{GS} = 0$)	V _{(BR)DSX}	25	-	Vdc
Zero-Gate-Voltage Drain Current $(V_{DS} = 10 \text{ V}, V_{GS} = 0) \text{ T}_A = 25^{\circ}\text{C}$ $T_A = 150^{\circ}\text{C}$	I _{DSS}	-	10 10	nAdc µAdc
Gate Reverse Current $(V_{GS} = \pm 15 \text{ Vdc}, V_{DS} = 0)$	I _{GSS}	-	± 10	pAdc
ON CHARACTERISTICS				
Gate Threshold Voltage $(V_{DS} = 10 \text{ V}, I_D = 10 \mu \text{A})$	V _{GS(Th)}	1.0	5	Vdc
Drain-Source On-Voltage ($I_D = 2.0 \text{ mA}, V_{GS} = 10V$)	V _{DS(on)}	-	1.0	v
On-State Drain Current ($V_{GS} = 10 \text{ V}, V_{DS} = 10 \text{ V}$)	I _{D(on)}	3.0	-	mAdo
SMALL-SIGNAL CHARACTERISTICS				
Forward Transfer Admittance ($V_{DS} = 10 \text{ V}, I_D = 2.0 \text{ mA}, f = 1.0 \text{ kHz}$)	y _{fs}	1000	=	µmho
Input Capacitance $(V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 140 \text{ kHz})$	C _{iss}	-	5.0	pF
Reverse Transfer Capacitance $(V_{DS} = 0, V_{GS} = 0, f = 140 \text{ kHz})$	C _{rss}	-	1.3	pF
Drain-Substrate Capacitance (V _{D(SUB)} = 10 V, f = 140 kHz)	C _{d(sub)}	~	5.0	pF
Drain-Source Resistance ($V_{GS} = 10 \text{ V}, I_D = 0, f = 1.0 \text{ kHz}$)	r _{ds(on)}	-	300	ohms
SWITCHING CHARACTERISTICS				
Turn-On Delay (Fig. 5)	t _{d1}	-	45	ns
Rise Time (Fig. 6) $I_D = 2.0 \text{ mAdc}, V_{DS} = 10 \text{ Vdc},$ (V _{GS} = 10 Vdc)	t _r		65	ns
Turn-Off Delay (Fig. 7) $(V_{GS} = 10 V_{GC})$ (See Figure 9; Times Circuit Determined)	t _{d2}	-	60	ns
fall Time (Fig. 8)	t _f		100	ns





MOSFETs are very sensitive to static electricity.

Because of the very thin SiO_2 layer between the external terminals and the layers of the device, any small electrical discharge can create an unwanted conduction.

Protection

- Always transport in a static sensitive bag
- Always wear a static strap when handling MOSFETS
- Apply voltage limiting devices between the gate and source, such as back-to-back Zeners to limit any transient voltage.



VMOS (vertical MOSFET) is a component structure that provides greater surface area.

Advantages

VMOS devices handle higher currents by providing more surface area to dissipate the heat.

VMOS devices also have faster switching times.



CMOS (complementary MOSFET) uses a p-channel and n-channel MOSFET; often on the same substrate as shown here.

Advantages

- Useful in logic circuit designs
- Higher input impedance
- Faster switching speeds
- Lower operating power levels