EE-202 Electronics-I-

Chapter 12:

JFET DC Biasing Circuits

Common FET Biasing Circuits

JFET

- Fixed – Bias
- Self-Bias
- Voltage-Divider Bias

Depletion-Type MOSFET

- Self-Bias
- Voltage-Divider Bias

Enhancement-Type MOSFET

- Feedback Configuration
- Voltage-Divider Bias

General Relationships

For all FETs:

$$I_G \cong 0A$$

$$I_D = I_S$$

For JFETS and depletion-type MOSFETs:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

For enhancement-type MOSFETs:

$$I_D = k(V_{GS} - V_T)^2$$

JFETs

JFETs are different from BJTs as;

- **Nonlinear relationship between input (V_{GS}) and output (I_D)**
- **JFETs , voltage controlled**
  BJTs, current controlled devices

Fixed-Bias Configuration

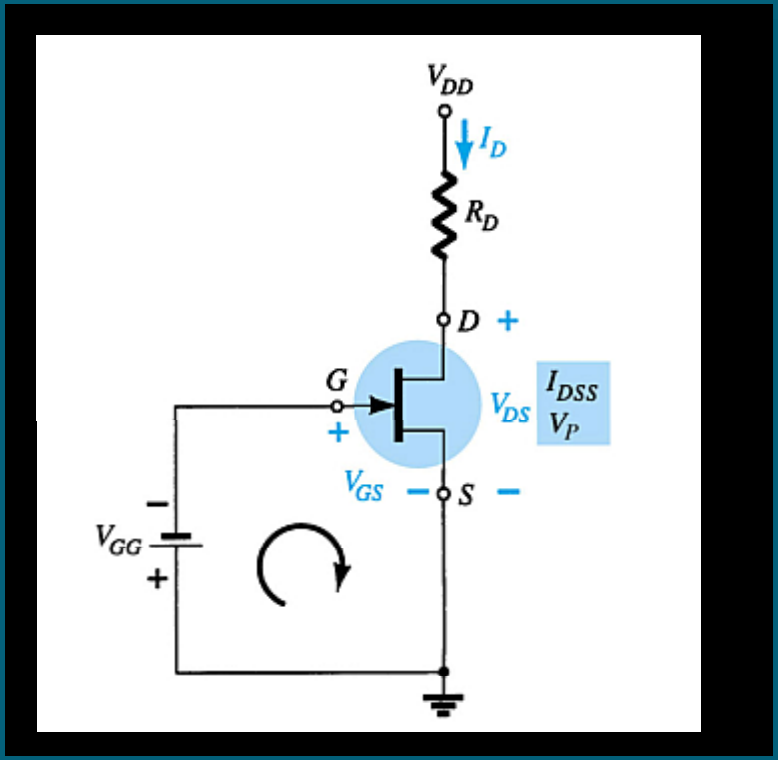
$V_{DS} = V_{DD} - I_D R_D$

$V_S = 0V$

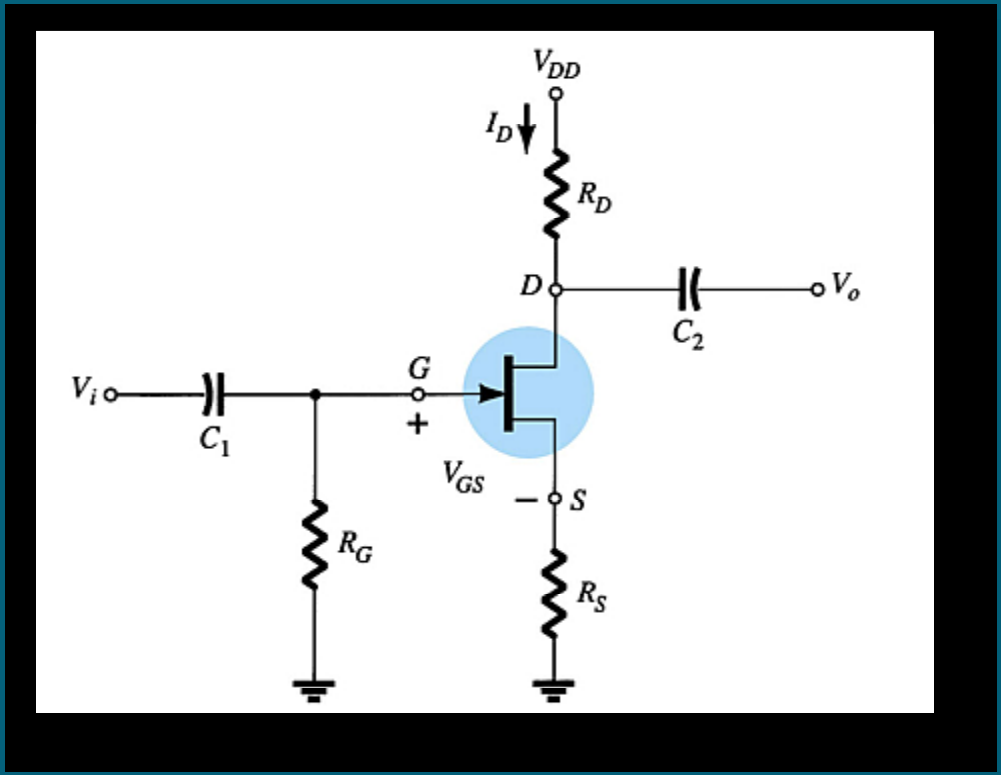
$V_C = V_{DS}$

$V = V_{GS}$

$V_{GS} = -V_{GG}$



Self-Bias Configuration



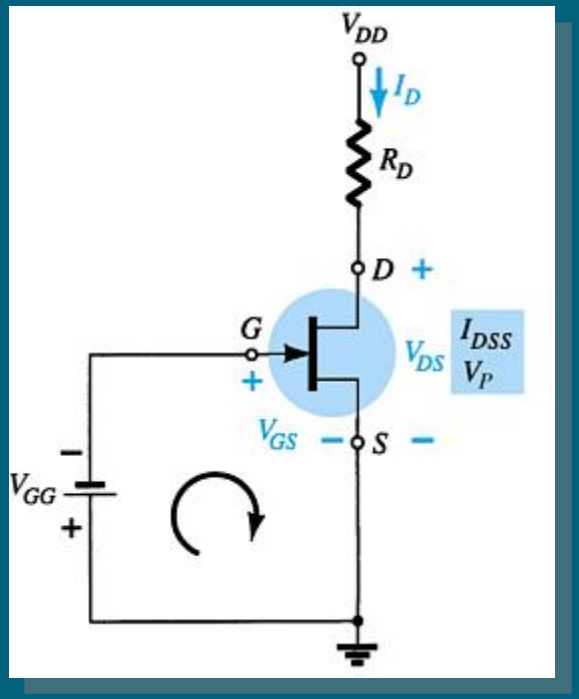
Self-Bias Calculations

$$V_{GS} = -I_D R_S$$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

$$V_S = I_D R_S$$

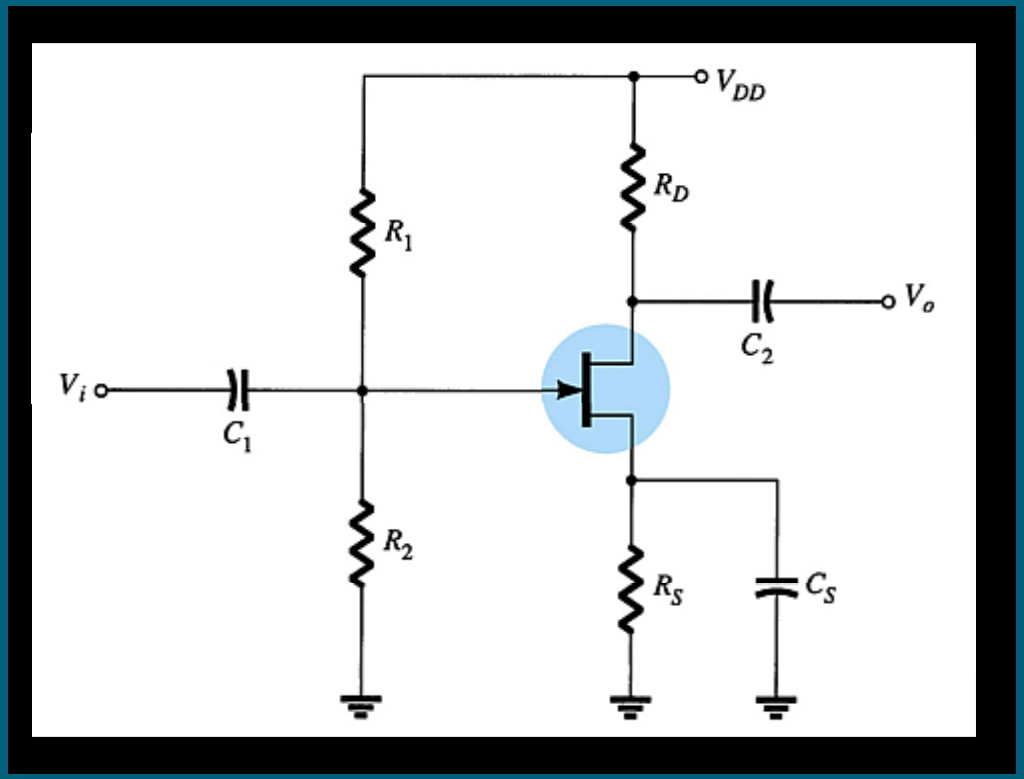
$$V_D = V_{DS} + V_S = V_{DD} - V_{RD}$$



Voltage-Divider Bias

$I_G = 0A$

-In BJTs, I_B affected I_C
-in FETs, V_{GS} controls I_D.



Voltage-Divider Bias Calculations

V_G is calculated by the voltage divider resistor R_2:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

By using Kirchhoff's Law:

$$V_{GS} = V_G - I_D R_S$$

By using Q-point values, the other variables in the voltage-divider bias circuit can be calculated as;

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$V_D = V_{DD} - I_D R_D$$

$$V_S = I_D R_S$$

$$I_{R1} = I_{R2} = \frac{V_{DD}}{R_1 + R_2}$$