
# BME 202 Electronics

## Lecture 5 : BJT – DC Biasing – Part 1

# Outline

- DC levels for basic BJT configurations
- Saturation and cutoff conditions
- Load-line analysis for basic BJT configurations
- Design process for BJT amplifiers
- Transistor swithcing networks

# Transistor Amplifier Analysis

Biasing: Applying DC voltages to a transistor in order to turn it on so that it can amplify AC signals.

*Any increase in AC voltage, current, or power is the result of a transfer of energy from the applied DC supplies*

$$V_{BE} \cong 0.7V$$

$$I_E = (\beta + 1)I_B \cong I_C$$

$$I_C = \beta I_B$$

# Biasing and Q-Point

The DC input establishes an operating or *quiescent point* called the ***Q-point*.**

Q-point selection?

- Small-signal amplification operation
- Power amplifier

Other Factors

- Temperature stability
- Stability factor

# The Three Operating Regions

## Active or Linear Region Operation

- Base–Emitter junction is forward biased
- Base–Collector junction is reverse biased

## Cutoff Region Operation

- Base–Emitter junction is reverse biased

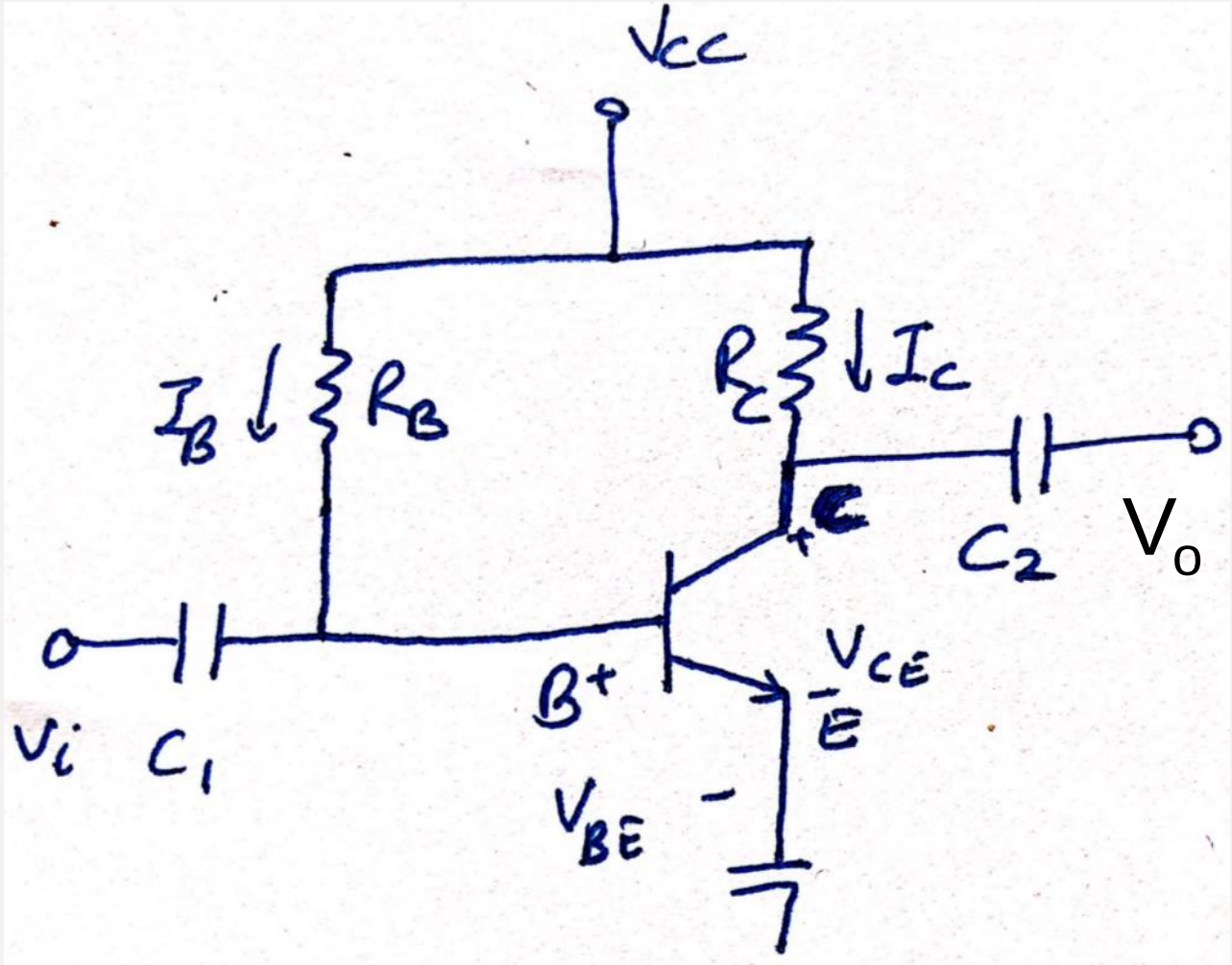
## Saturation Region Operation

- Base–Emitter junction is forward biased
- Base–Collector junction is forward biased

# DC Biasing Circuits

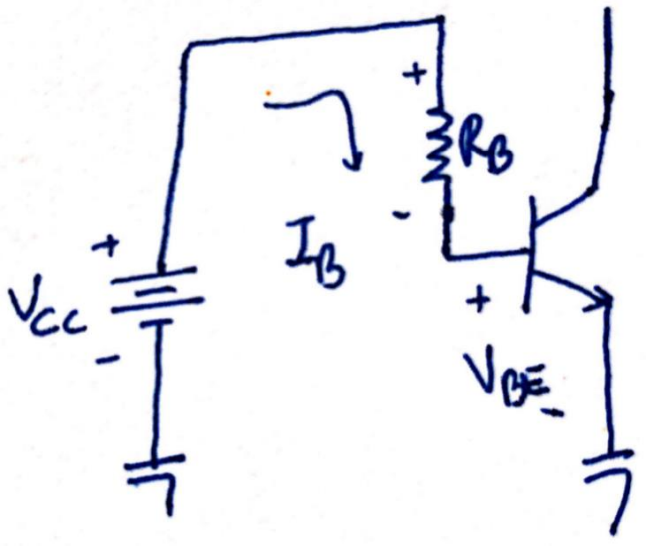
- Fixed-bias configuration
- Emitter bias configuration
- Voltage divider bias configuration
- Collector feedback configuration
- Common-base configuration
- Miscellaneous bias configurations

# Fixed Bias



# Fixed Bias

## The Base-Emitter Loop




From KVL:

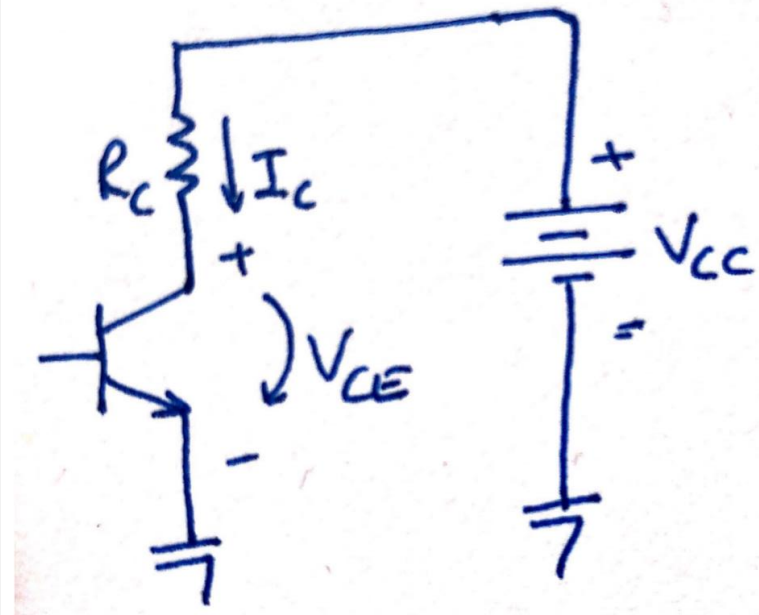
$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Solving for base current:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

# Fixed Bias

## The Collector-Emitter Loop



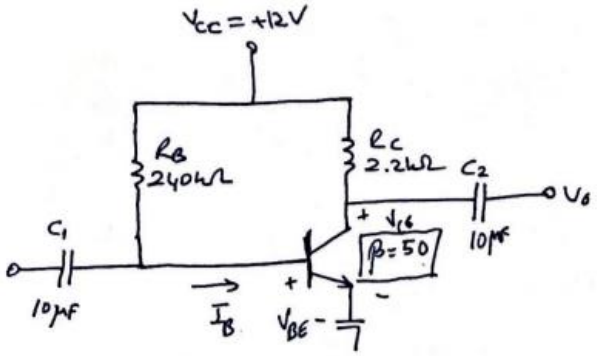

Collector current:

$$I_C = \beta I_B$$

From KVL:

$$V_{CE} = V_{CC} - I_C R_C$$

# Example




Determine $I_B$, $I_{CQ}$, $V_{CEQ}$, $V_B$, $V_C$ and $V_{BC}$

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12V - 0.7V}{240k\Omega} \cong 47.08\,\mu A$$

$$I_{CQ} = \beta I_B = 50.(47.08\,\mu A) = 2.35mA$$

$$V_{CC} - I_C R_C - V_{CEQ} = 0$$

$$V_{CEQ} = V_{CC} - I_C R_C = 12V - (2.35mA)(2.2k\Omega) = 6.38V.$$

$$V_B = V_{CC} - I_C R_C = 12V - (240k\Omega)(47.08\,\mu A) = 0.7V = V_{BE}$$

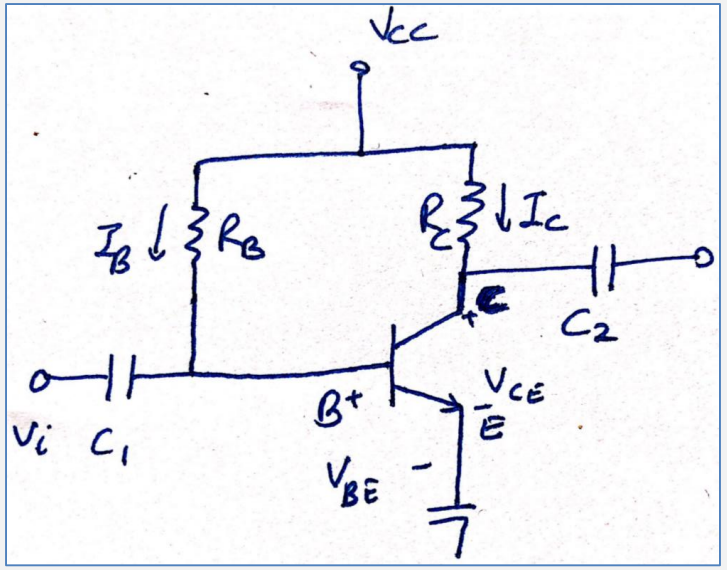
$$V_C = V_{CEQ} = 6.38V \quad , V_{BC} = V_B - V_C = 0.7V - 6.85V = -6.13V$$

# Fixed Bias

## Saturation

When the transistor is operating in *saturation*, current through the transistor is at its *maximum* possible value.

$$I_{Csat} = \frac{V_{CC}}{R_C} \qquad V_{CE} \cong 0\ V$$



# Fixed Bias

## Load-Line Analysis

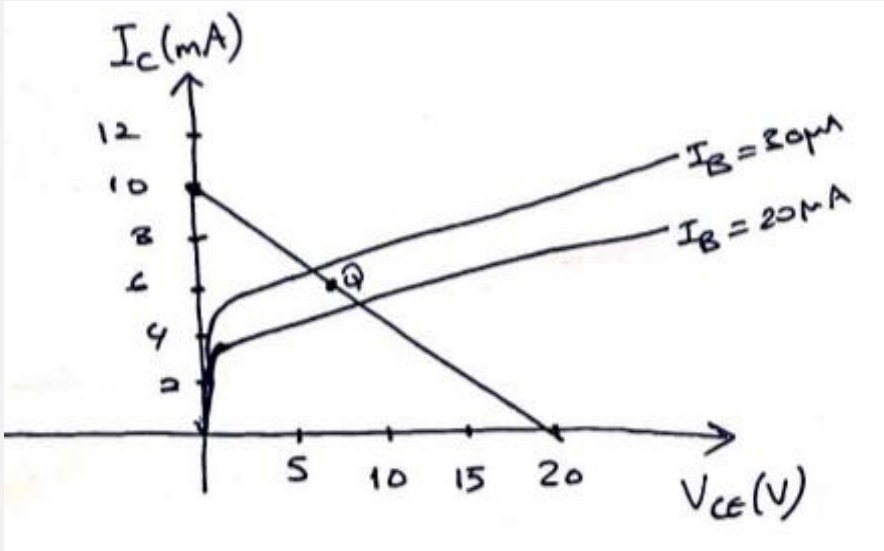
The load line end points are:

$I_{Csat}$

$$I_C = V_{CC} / R_C$$
$$V_{CE} = 0 \text{ V}$$

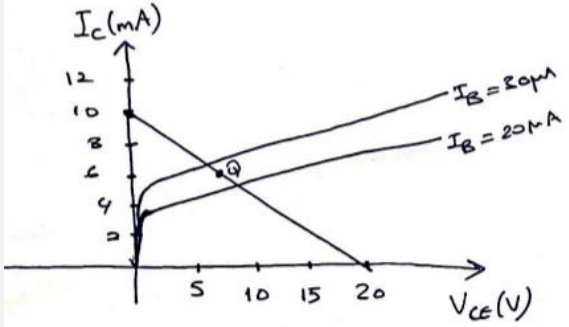
$V_{CEcutoff}$

$$V_{CE} = V_{CC}$$
$$I_C = 0 \text{ mA}$$




The *Q*-point is the operating point where the value of $R_B$ sets the value of $I_B$ that controls the values of $V_{CE}$ and $I_C$.

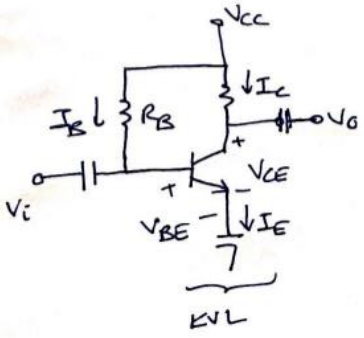
# Example




Given the load line and the defined Q point, determine:

$V_{CC}$, $R_C$ and $R_B$ for a fixed-bias conf.

Remember Fixed-Bias Conf:




KVL: $V_{CC} - I_C R_C - V_{CE} = 0$

$V_{CE} = V_{CC} - I_C R_C$

When $I_C = 0 \Rightarrow V_{CE} = V_{CC} = 20V$.

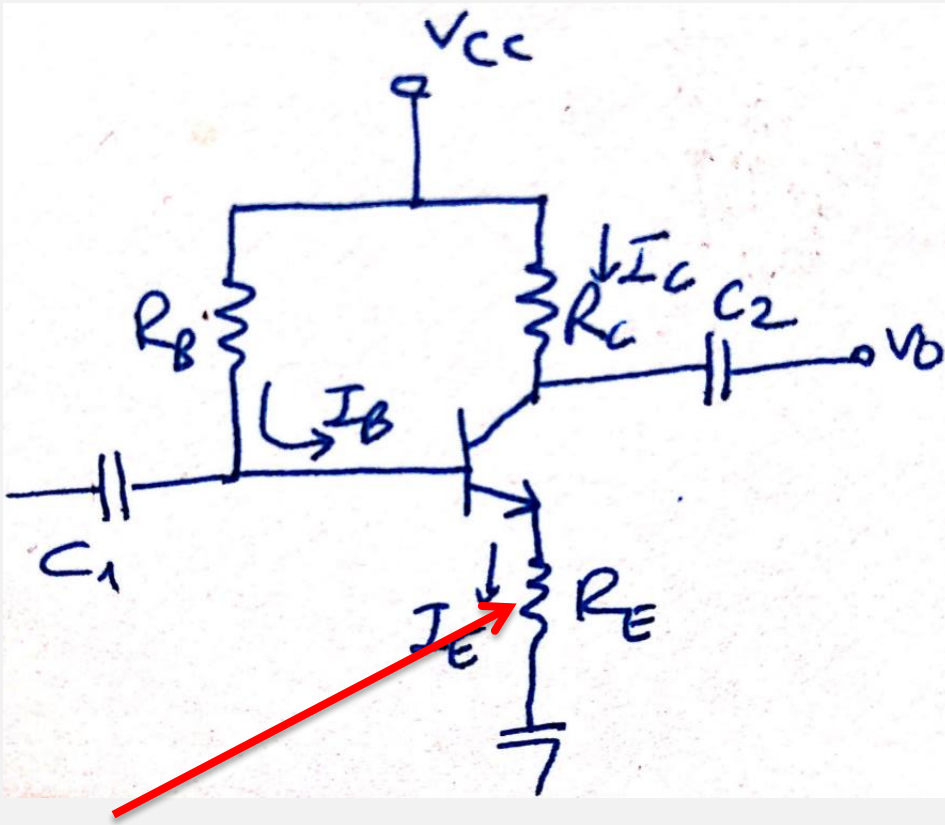
When $V_{CE} = 0V \Rightarrow I_C R_C = V_{CC} \Rightarrow R_C = \frac{20V}{10mA} = 2k\Omega$

From Q Point : $I_B \cong 25\mu A$

$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{20V - 0.7V}{R_B} \Rightarrow R_B = \frac{19.3V}{25\mu A} = 772\,k\Omega$

# Emitter Bias Circuit

Adding a resistor ($R_E$) to the emitter circuit stabilizes the bias circuit.
$\rightarrow$ its response will change less due to undesirable changes in temperature and other parameters.



# Emitter Bias Circuit

## Base-Emitter Loop

From KVL:

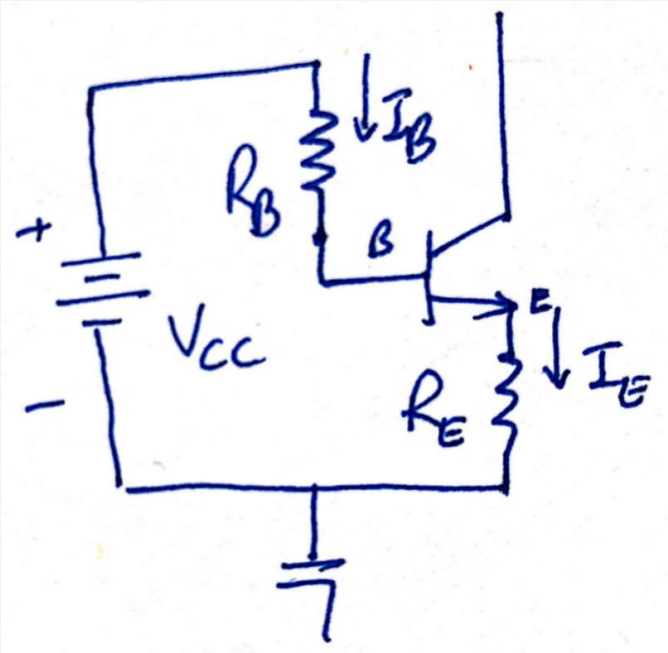
$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

Since $I_E = (\beta + 1) I_B$:

$$V_{CC} - V_{BE} - (\beta + 1) I_B R_E = 0$$

Solving for $I_B$:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$



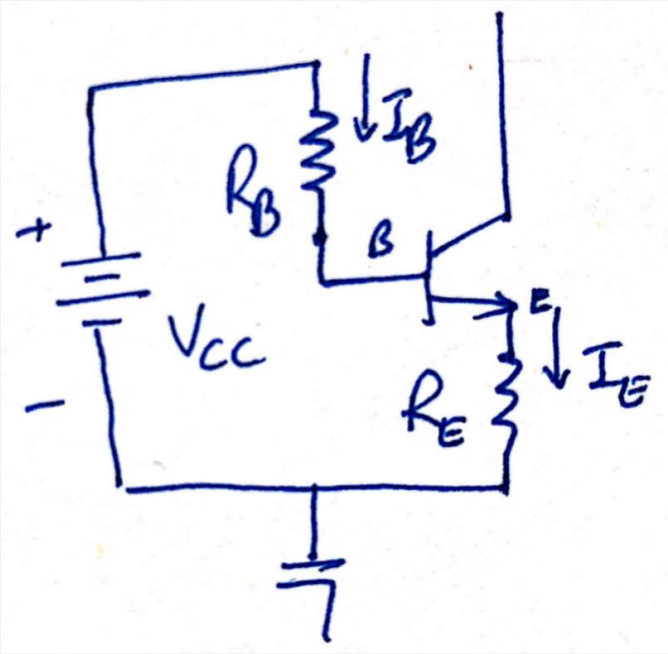
# Emitter Bias Circuit

## Effect of $R_E$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$R_E$ is reflected back to input base current by a factor $(\beta + 1)$

$$R_i = (\beta + 1)R_E$$



# Emitter Bias Circuit

## Collector-Emitter Loop

From KVL:

$$I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Since $I_E \cong I_C$:

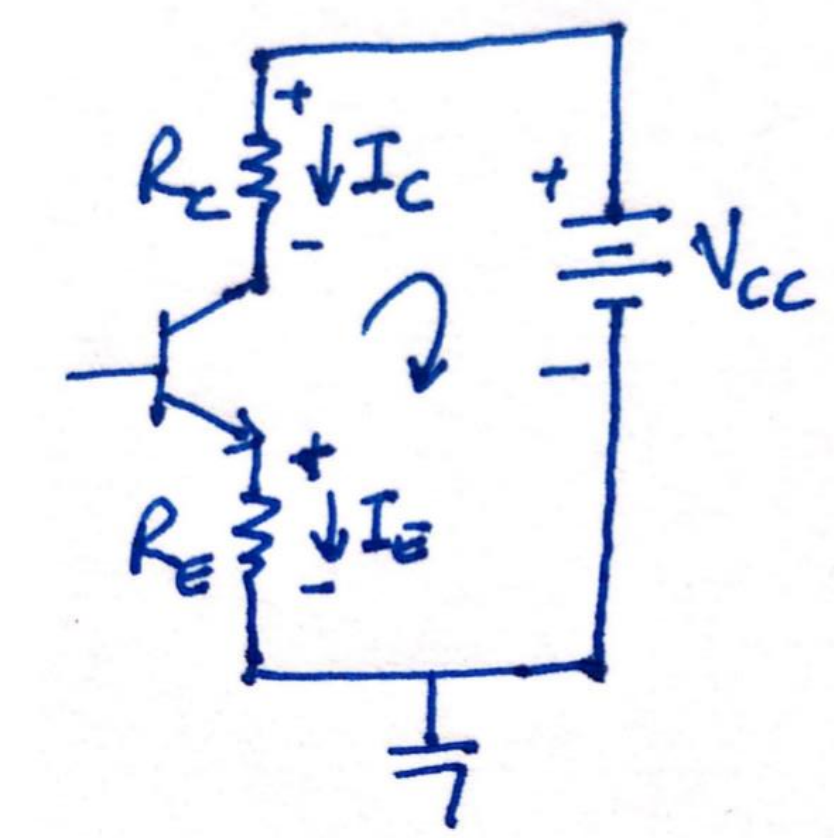
$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

and:

$$V_E = I_E R_E$$

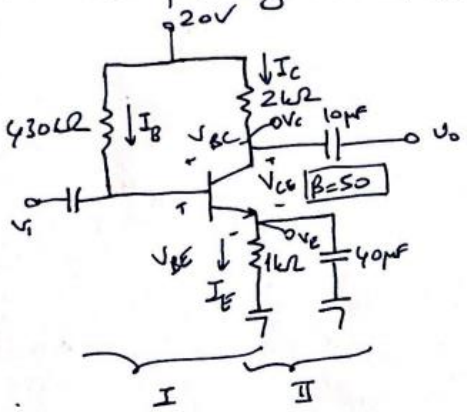
$$V_C = V_{CE} + V_E = V_{CC} - I_C R_C$$

$$V_B = V_{CC} - I_R R_B = V_{BE} + V_E$$



# Example

For the following circuit, determine $I_B, I_C, V_{CE}, V_C, V_E, V_B, V_{BC}$




I) $20V - (430k\Omega)I_B - V_{BE} - (\beta+1)R_E I_B = 0$

$I_B\,(430k\Omega + (51)(1k\Omega)) = 20V - 0.7V$

$I_B = \dfrac{19.3V}{481k\Omega} = 40.1\mu A \Rightarrow I_C = \beta I_B = 50(40.1\mu A) = 2.01mA$

II) $I_E \approx I_C$

$20V - (2k\Omega)I_C - V_{CE} - (1k\Omega)I_C = 0$

$V_{CE} = 20V - I_C(3k\Omega) \overset{I_C \approx 2.01mA}{=} 13.97V$

$V_C = 20V - (2k\Omega)I_C = 20V - 4.02V = 15.98V$

$V_E = 1k\Omega\, I_C = (2.01mA)(1k\Omega) = 2.01V$

$V_B = V_E + V_{BE} = 2.01V + 0.7V = 2.71V$

$V_{BC} = V_B - V_C = 2.71V - 15.98V = -13.27V$

# Emitter Bias Circuit

## Improved Biased Stability

Stability refers to a condition in which the currents and voltages remain fairly constant over a wide range of temperatures and transistor Beta ($\beta$) values.

Adding $R_E$ to the emitter improves the stability of a transistor.

Example: change $\beta$ from 50 to 100 and compare with fixed bias.

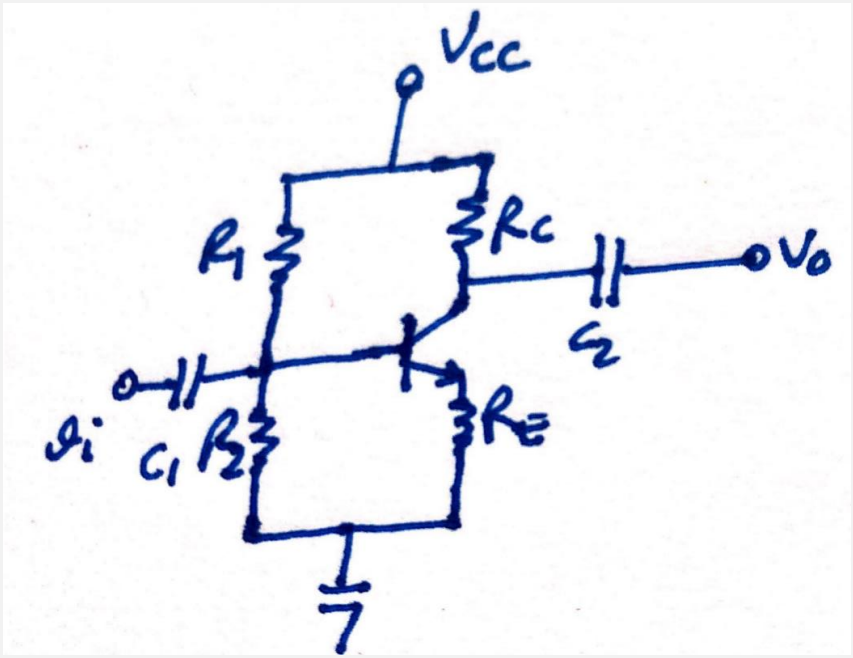
Fixed-Bias

| $\beta$ | $I_B$ (μA) | $I_C$ (mA) | $V_{CE}$(V) |
|---|---|---|---|
| 50 | 47.08 | 2.35 | 6.83 |
| 100 | 47.08 | 4.71 | 1.64 |

Emitter-Bias

| $\beta$ | $I_B$ (μA) | $I_C$ (mA) | $V_{CE}$(V) |
|---|---|---|---|
| 50 | 40.1 | 2.01 | 13.97 |
| 100 | 36.3 | 3.63 | 9.11 |

# Voltage Divider Bias



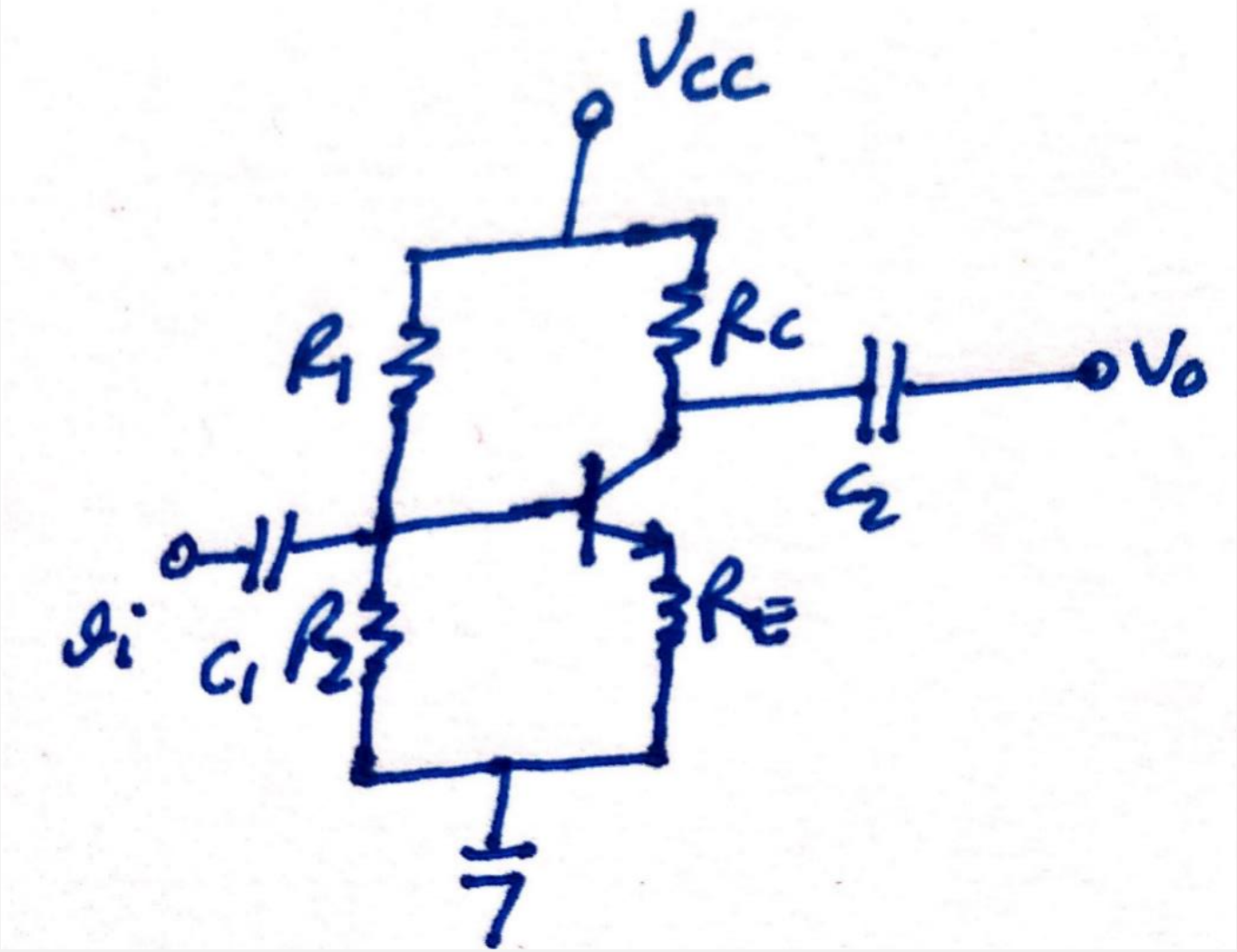

The currents and voltages are nearly independent of any variations in $\beta$.

*A very stable bias circuit.*

Exact Analysis

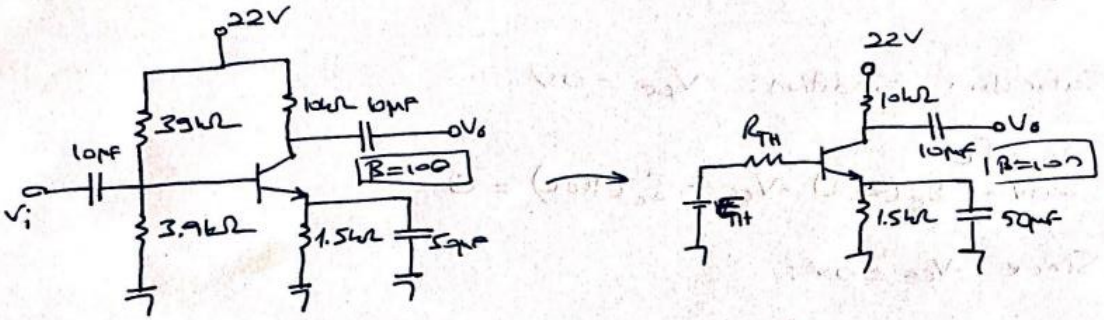
Approximate Analysis

# Voltage Divider Bias *Exact Analysis*



# Example

Determine $V_{CE}$ and $I_C$ for the following circuit:




$$R_{TH} = R_1 \| R_2 = (39\,k\Omega) \| (3.9\,k\Omega) = 3.55\,k\Omega$$

$$E_{TH} = \frac{R_2 V_{CC}}{(R_1 + R_2)} = \frac{(3.9\,k\Omega)(22V)}{(39\,k\Omega + 3.9\,k\Omega)} = 2V$$

$$I_B = \frac{E_{TH} - V_{BE}}{R_{TH} + (\beta+1)R_E} = \frac{2V - 0.7V}{(3.55\,k\Omega) + (101)(1.5\,k\Omega)} = \frac{1.3V}{(3.55\,k\Omega) + (151.5\,k\Omega)}$$

$$= 8.38\,\mu A$$

$$I_C = \beta I_B$$

$$= 100 \cdot (8.38\,\mu A)$$

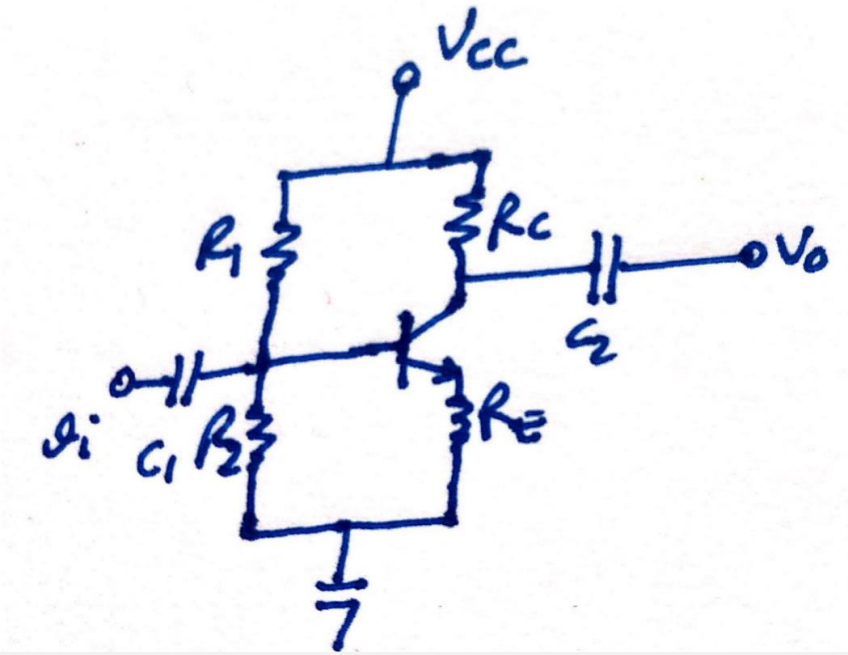
$$= 0.84\,mA$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 22V - 0.84mA\,(10k\Omega + 1.5k\Omega)$$

$$= 12.34V$$

# Voltage Divider Bias *Approximate Analysis*




$I_B << I_1$ and $I_1 \cong I_2$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$\beta R_E > 10R_2$:

$$I_E = \frac{V_E}{R_E}$$

$$V_E = V_B - V_{BE}$$

using Kirchhoff's voltage law:

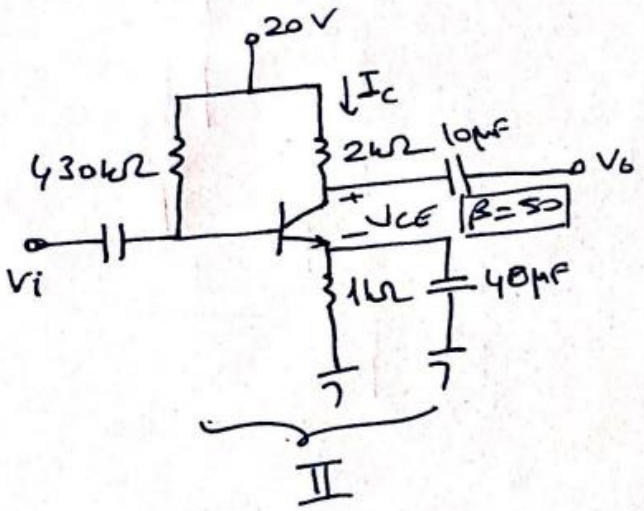
$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$I_E \cong I_C$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

# Example

Determine $I_{csat}$ of the following circuit:




Saturation condition: $V_{CE} = 0V$.

$I_C \approx I_E$

II) $20V - I_C(2k\Omega) - V_{CE} - I_e(1k\Omega) = 0$

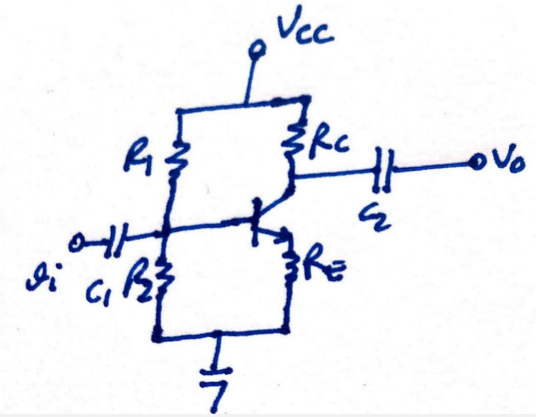
Since $V_{CE} = 0V$:

$20V = I_C(3k\Omega)$

$I_{CQ} = I_{Csat} = \frac{20V}{3k\Omega} = 6.67\,mA$

# Voltage Divider Bias

## Transistor Saturation Level




$$I_{Csat} = I_{C\max} = \frac{V_{CC}}{R_C + R_E}$$

## Load Line Analysis

### Cutoff

$$V_{CE} = V_{CC}$$

$$I_C = 0\ mA$$

### Saturation

$$I_C = \frac{V_{CC}}{R_C + R_E}$$

$$V_{CE} = 0\ V$$

# Summary

## DC Biasing Configurations

- Fixed-bias configuration
- Emitter bias configuration
- Voltage divider bias configuration
- Collector feedback configuration
- Common-base configuration
- Miscellaneous bias configurations

Part 1

Part 2