BME 202 Electronics

Lecture 6: BJT – DC Biasing – Part 2

Outline

- DC levels for basic BJT configurations
- Saturation and cutoff conditions
- Load-line analysis for basic BJT configurations
- Design process for BJT amplifiers
- Transistor swithcing networks

DC Biasing Circuits

- Fixed-bias configuration
- Emitter bias configuration
- Voltage divider bias configuration

Part 1

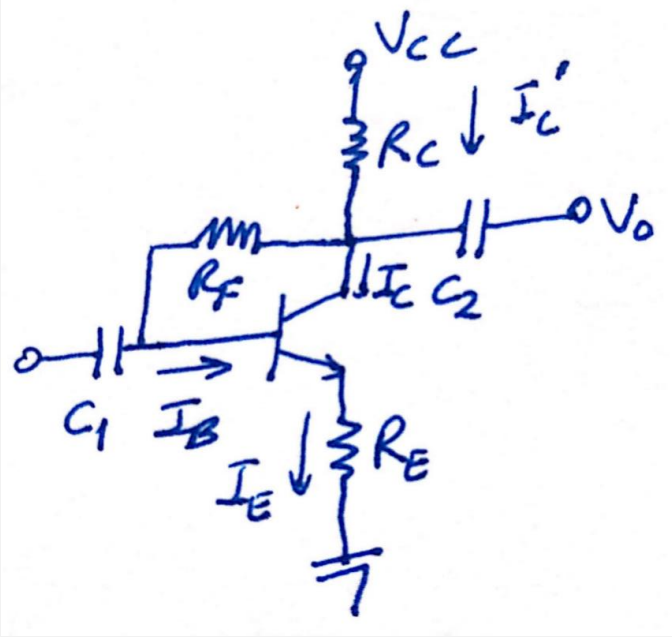
- Collector feedback configuration
- Common-base configuration
- Miscellaneous bias configurations

Part 2

Collector Feedback Configuration

Another way to improve the stability of a bias circuit is to add a feedback path from collector to base.

In this bias circuit the Q-point is slightly dependent on the transistor beta, β.



Collector Feedback Configuration

Base-Emitter Loop

From KVL

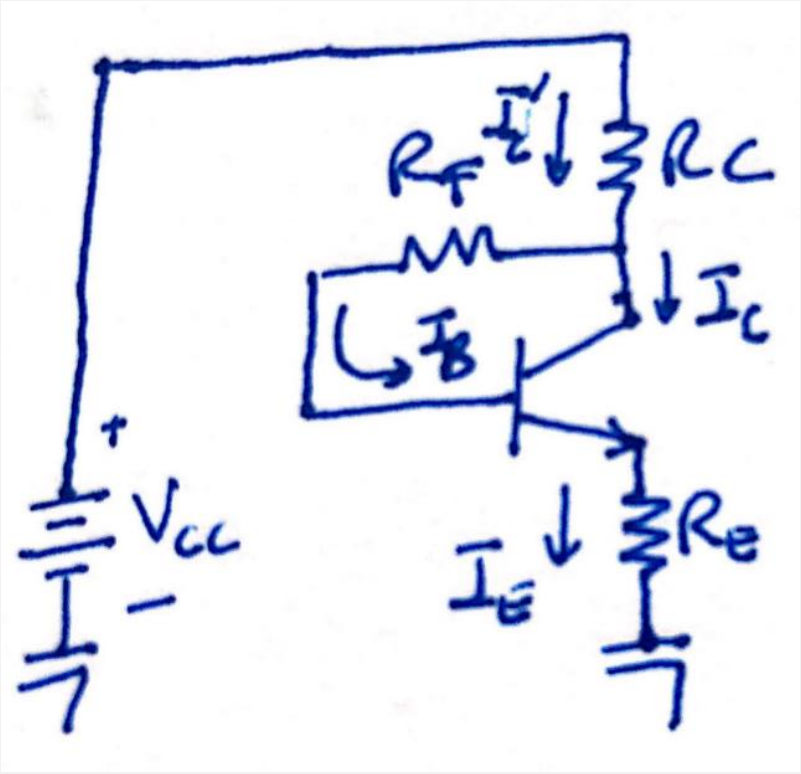
$$V_{CC} - I'_C R_C - I_B R_F - V_{BE} - I_E R_E = 0$$

$I_B << I_C$ $\qquad I'_C = I_C + I_B \cong I_C$

Having $I_C = \beta I_B$ and $I_E \cong I_C$, the loop equation becomes:

$$V_{CC} - \beta I_B R_C - I_B R_F - V_{BE} - \beta I_B R_E = 0$$

Solving for I_B: $\qquad I_B = \dfrac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}$



Collector Feedback Configuration

Collector-Emitter Loop

Applying KVL:

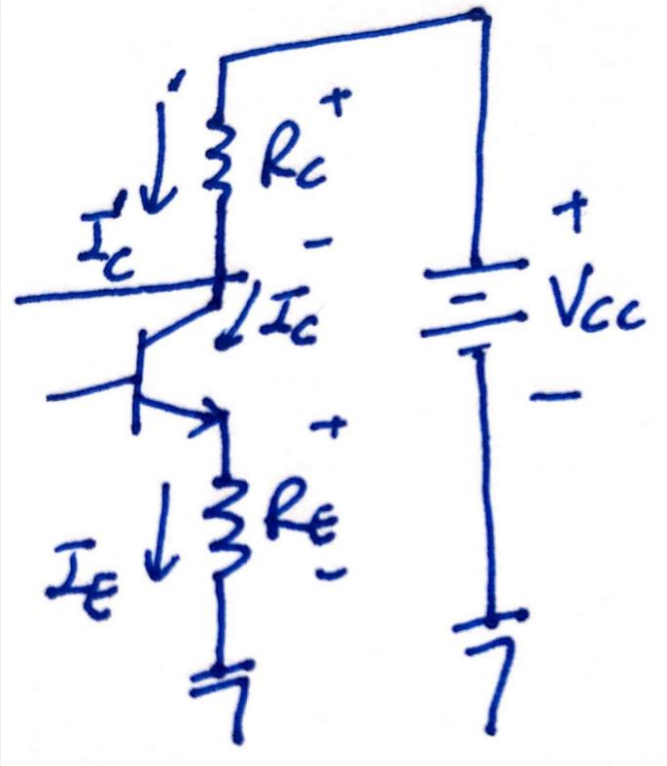
$$I_E + VCE + I'_C R_C - VCC = 0$$

Since $I'_C \cong I_C$ and $I_C = \beta I_B$:

$$I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$$

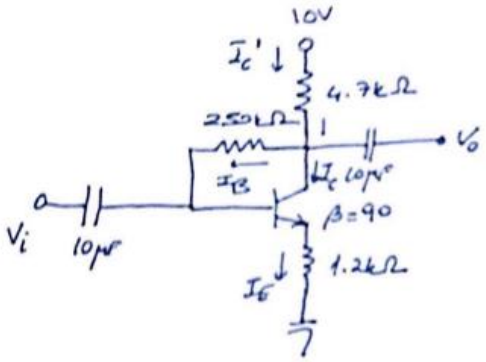
Solving for V_{CE}:

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$



Exactly the same as voltage divider bias

Examples



Determine the quiescent levels of I_{CQ} and V_{CEQ} for the network given on the left.

I. KVL

$$I_C' = I_E \cong I_C = \beta I_B$$

$$10V - \beta(4.7k\Omega)I_B - (250k\Omega)I_B - V_{BE} - \beta(1.2k\Omega)I_B = 0$$

$$I_B = \frac{10V - 0.7V}{(250k\Omega) + \beta(4.7k\Omega + 1.2k\Omega)} = \frac{9.3V}{(250k\Omega + 531k\Omega)} = \frac{9.3V}{781k\Omega}$$

$$I_B = 11.91\,\mu A$$

$$I_{CQ} = \beta I_B = 90\,(11.91\,\mu A) = 1.07\,mA$$

II. KVL

$$I_C \cong I_E$$

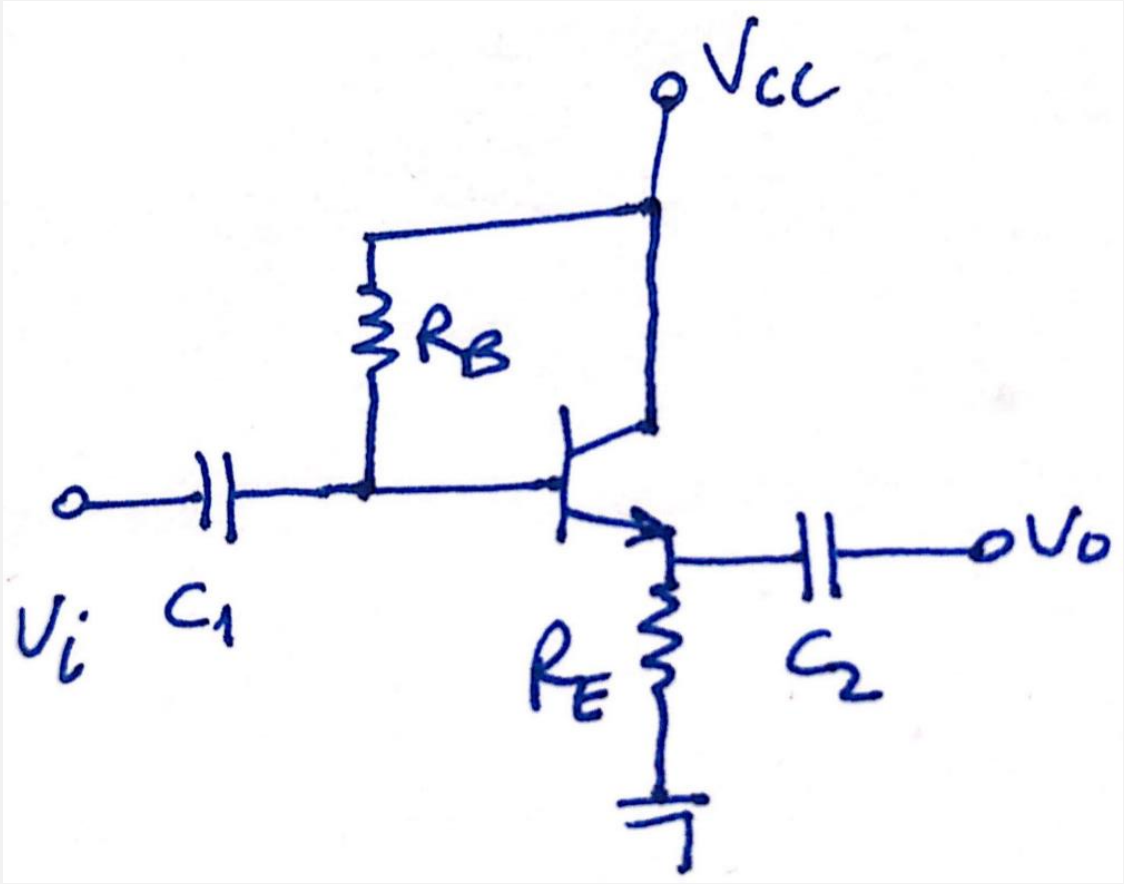
$$10V - (4.7k\Omega)I_C - V_{CEQ} - (1.2k\Omega)I_C = 0$$

$$V_{CEQ} = 10V - (1.07mA)(4.7k\Omega + 1.2k\Omega)$$

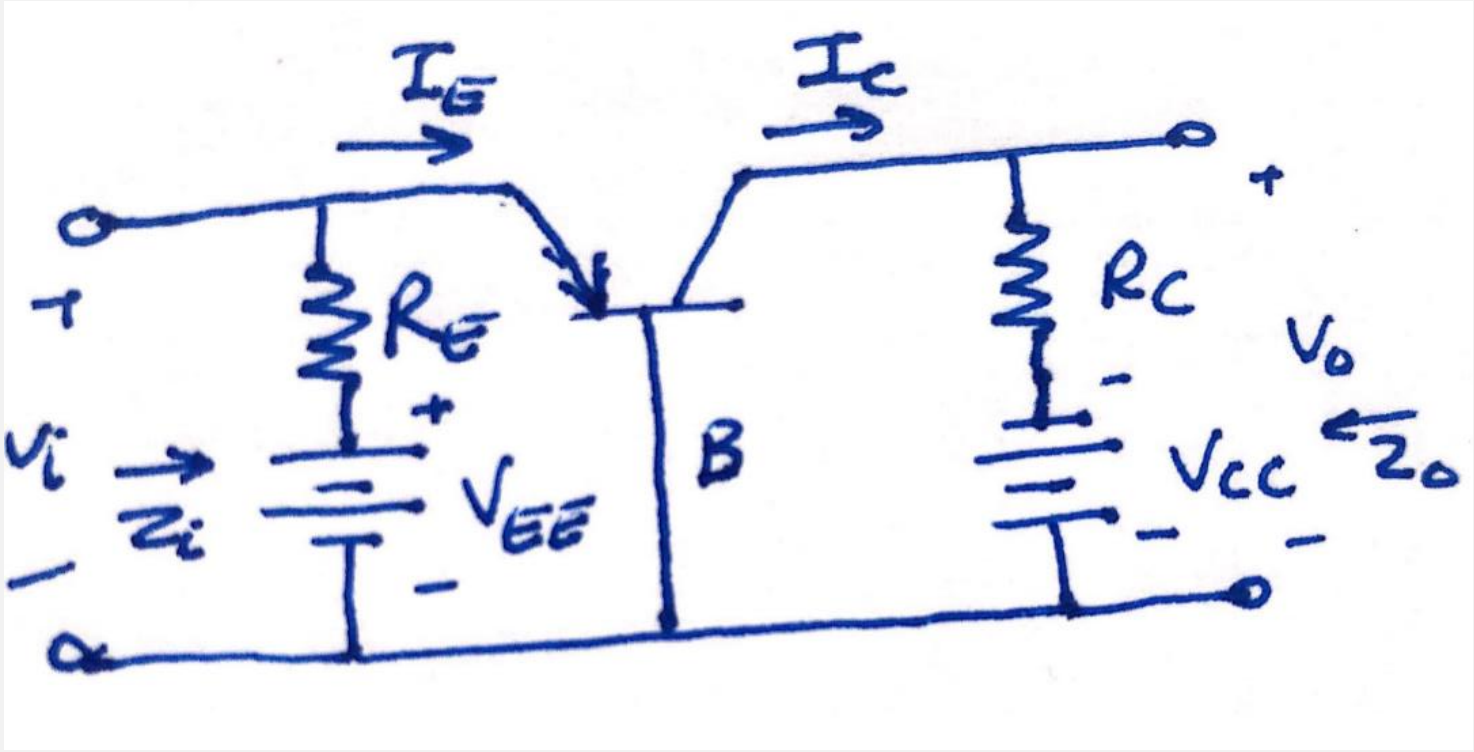
$$= 10V - 6.31V$$

$$V_{CEQ} = 3.69V$$

Emitter-Follower



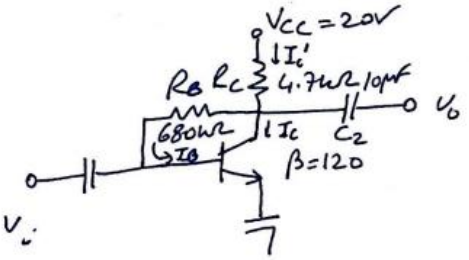
Common-Base Configuration



Miscellaneous Bias Configurations

For the network given below:

- Determine I_{CQ} and V_{CEQ}
- Find V_B, V_C, V_E and V_{BC}



I KVL : $I_C' \cong I_C = \beta I_B$

$$20V - (4.7k\Omega)\beta I_B - (680k\Omega) I_B - V_{BE} = 0$$

$$I_B = \frac{20V - 0.7V}{(\beta 4.7k\Omega) + 680k\Omega} = \frac{19.3V}{1.244M\Omega} = \boxed{15.51\mu A}$$

$$I_{CQ} = \beta I_B = \boxed{1.86mA}$$

II KVL : $I_C' \cong I_C$

$$20V - (4.7k\Omega) I_C - V_{CEQ} = 0$$

$$V_{CEQ} = 20V - (1.86mA)(4.7k\Omega) = \boxed{11.26V}$$

$$V_B = V_{BE} = \boxed{0.7V}$$

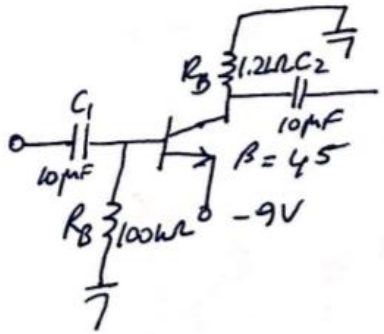
$$V_C = V_{CE} = \boxed{11.26V}$$

$$V_E = \boxed{0}$$

$$V_{BC} = V_B - V_C = 0.7V - 11.26V = \boxed{-10.56V}$$

Miscellaneous Bias Configurations

Determine V_C and V_B for the network given below:



I. KVL

$$(-100k\Omega)I_B - V_{BE} + 9V = 0$$

$$I_B = \frac{9V - 0.7V}{100k\Omega} = \underline{83\mu A}$$

$$I_C = \beta I_B = \underline{3.735\,mA}$$

$$0 - (1.2k\Omega)I_C - V_{CE_Q} + 9V = 0$$

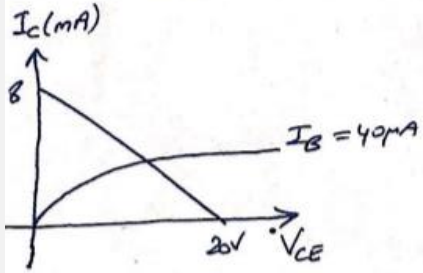
$$V_{CE_Q} = 9V - (1.2k\Omega)(3.735mA) = 4.52V$$

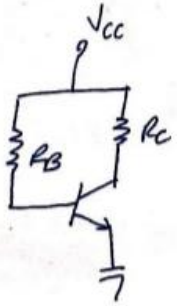
$$V_C = -I_C R_C = \boxed{-4.48V}$$

$$V_B = -I_B R_B = \boxed{-8.3V}$$

Design Examples

Given the device characteristics given below and the fixed bias configuration, determine V_{CC}, R_B, and R_C:





From the load line : $V_{CC} = 20V$

$$I_C = \frac{V_{CC}}{R_C}\Big|_{V_{CE}=0V}$$

$$R_C = \frac{V_{CC}}{I_C} = \frac{20V}{8mA} = 2.5k\Omega$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \Rightarrow R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

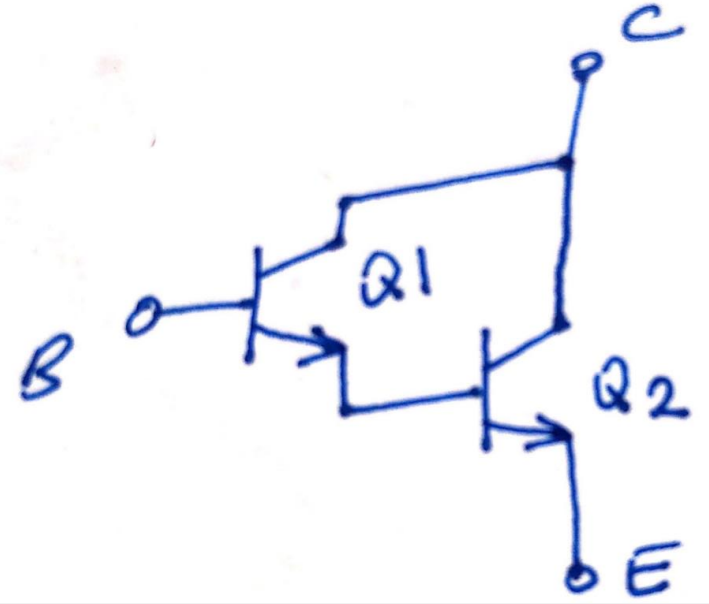
$$R_B = \frac{20V - 0.7V}{40\mu A} = \frac{19.3V}{40\mu A} = 482.5k\Omega$$

Multiple BJT Networks

Cascaded Systems

- The output of one amplifier is the input to the next amplifier
- The overall voltage gain is determined by the product of gains of the individual stages
- The DC bias circuits are isolated from each other by the coupling capacitors
- The DC calculations are independent of the cascading
- The AC calculations for gain and impedance are interdependent

Darlington Connection

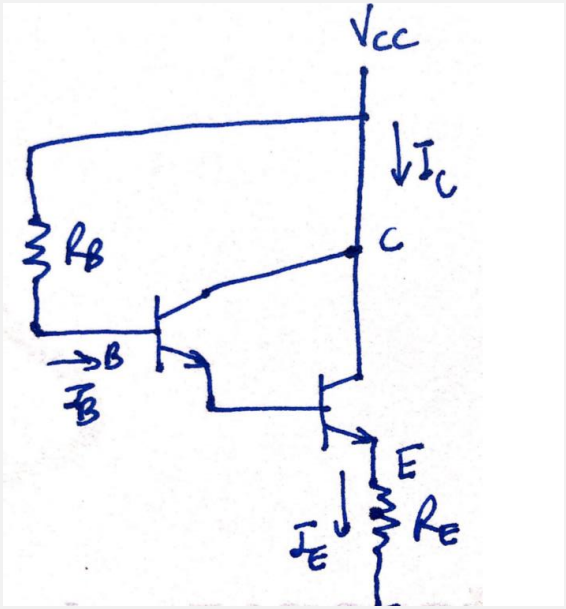


The Darlington circuit provides very high current gain, equal to the product of the individual current gains:

$$\beta_D = \beta_1 \beta_2$$

The practical significance is that the circuit provides a very high input impedance.

DC Bias of Darlington Circuits



Base current:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta_D R_E}$$

Emitter current:

$$I_E = (\beta_D + 1) I_B \cong \beta_D I_B$$

Emitter voltage:

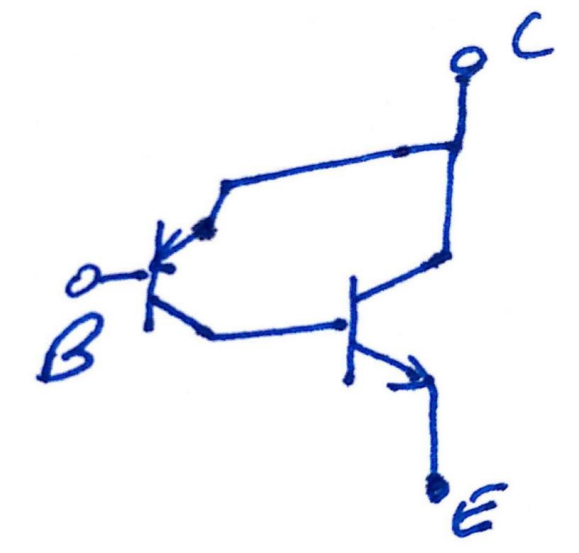
$$V_E = I_E R_E$$

Base voltage:

$$V_B = V_E + V_{BE}$$

Feedback Pair

This is a two-transistor circuit that operates like a Darlington pair, *but it is not a Darlington pair*.

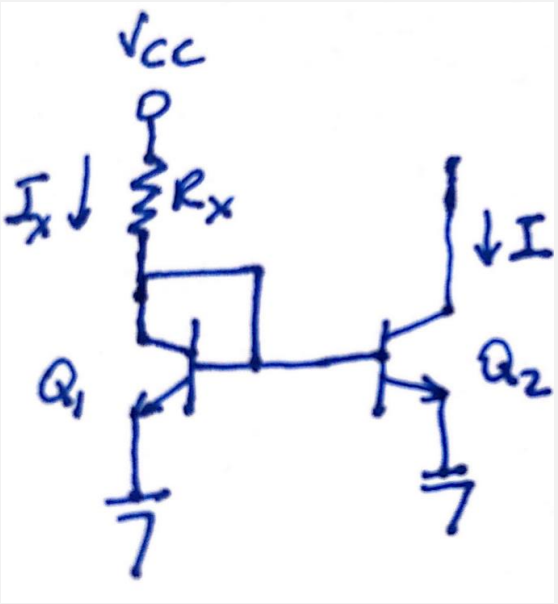


It has similar characteristics:

- High current gain
- Voltage gain near unity
- Low output impedance
- High input impedance

The difference is that a Darlington uses a pair of like transistors, whereas the feedback-pair configuration uses complementary transistors.

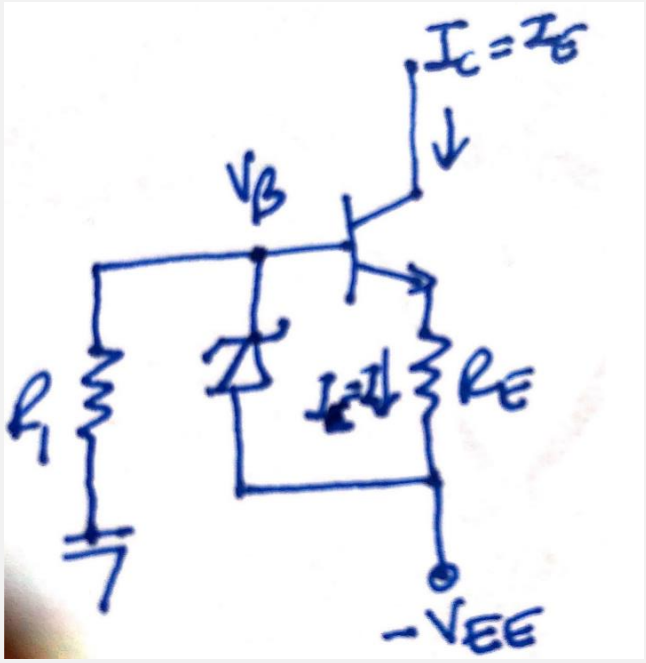
Current Mirrors

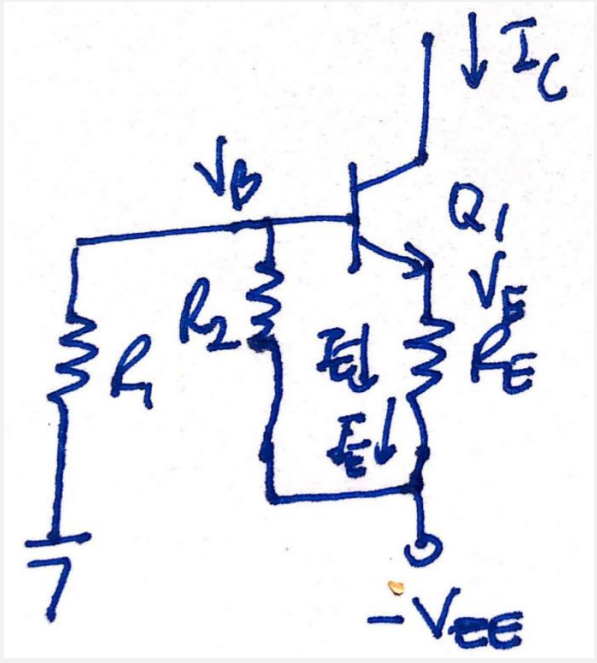


Current mirror circuits provide constant current in integrated circuits.

Current Source Circuits

Constant-current sources can be built using FETs, BJTs, and combinations of these devices.





$$I \cong I_E = \frac{V_Z - V_{BE}}{R_E}$$

$$I_E \cong I_C$$

PNP Transistors

The analysis for *pnp* transistor biasing circuits is the same as that for *npn* transistor circuits. The only difference is that the currents are flowing in the opposite direction.