BME 202 Electronics

Lecture 9: Field Effect Transistors – Part 1

FETs vs. BJTs

Similarities:

Amplifiers
Switching devices
Impedance matching circuits

Differences:

FETs are voltage controlled devices. BJTs are current controlled devices.

FETs have higher input impedance. BJTs have higher gain.

FETs are less sensitive to temperature variations and are better suited for integrated circuits

FETs are generally more static sensitive than BJTs.

FET Types

JFET: Junction FET

MOSFET: Metal–Oxide–Semiconductor FET

D-MOSFET: Depletion MOSFET

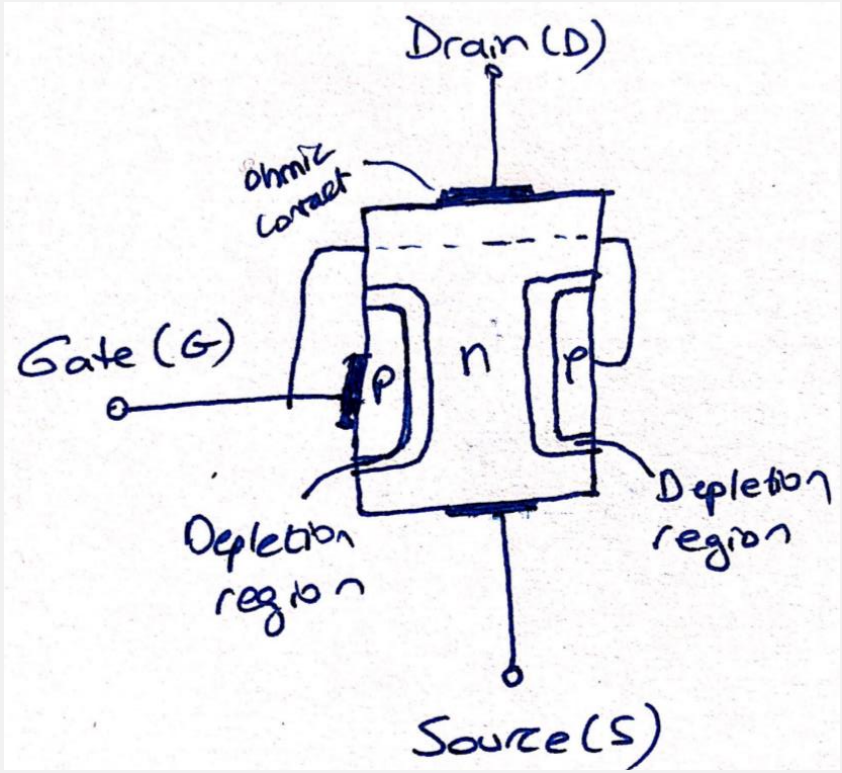
E-MOSFET: Enhancement MOSFET

JFET Construction

There are two types of JFETs:

***n*-channel**
***p*-channel**

The n-channel is the more widely used of the two.



JFETs have three terminals:

The **Drain** (D) and **Source** (S) are connected to the *n*-channel

The **Gate** (G) is connected to the *p*-type material

JFET Operation: The Basic Idea

JFET operation can be compared to that of a water spigot.

The source is the accumulation of electrons at the negative pole of the drain-source voltage.

The drain is the electron deficiency (or holes) at the positive pole of the applied voltage.

The gate controls the width of the n-channel and, therefore, the flow of charges from source to drain.

JFET Operating Characteristics

There are three basic operating conditions for a JFET:

- V_{GS} = 0 V, V_{DS} increasing to some positive value
- V_{GS} < 0 V, V_{DS} at some positive value
- Voltage-controlled resistor

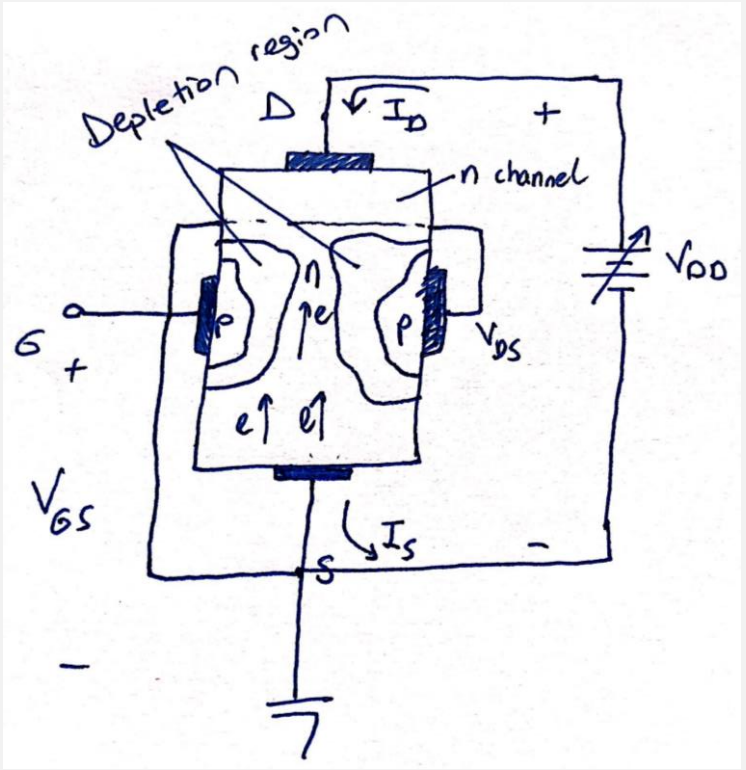
JFET Characteristics: V_{GS}=0V

Three things happen when V_{GS} = 0 V and V_{DS} increases from 0 V to a more positive voltage:

- The size of the depletion region between *p*- type gate and *n*-channel increases.

- Increasing the size of the depletion region decreases the width of the *n*-channel, which increases its resistance.

- Even though the *n*-channel resistance is increasing, the current from source to drain (I_D) through the *n*-channel is increasing because V_{DS} is increasing.



JFET Characteristics: Pinch Off

- If V_{GS} = 0 V and V_{DS} continually increases to a more positive voltage, a point is reached where the depletion region gets so large that it pinches off the channel.

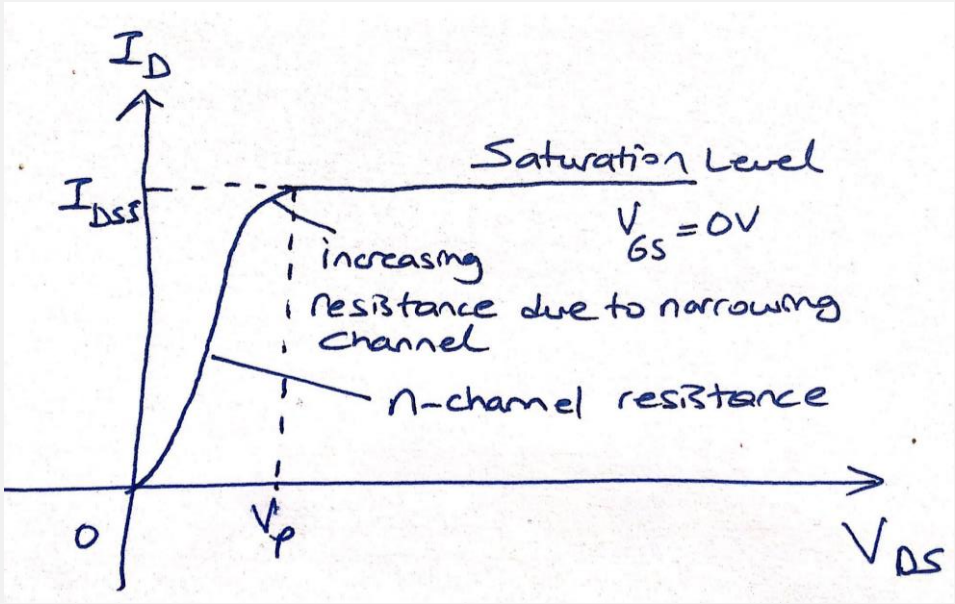
- This suggests that the current in channel (I_D) drops to 0 A, but it does not: As V_{DS} increases, so does I_D. However, once pinch off occurs, further increases in V_{DS} do not cause I_D to increase.

JFET Characteristics: Saturation

At the pinch-off point:

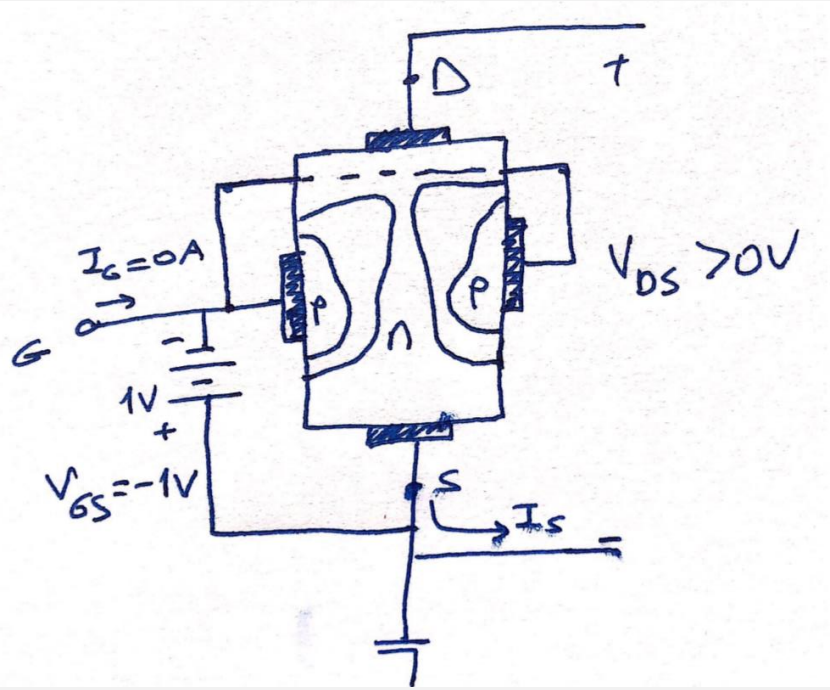
Any further increase in V_{DS} does not produce any increase in I_D. V_{DS} at pinch-off is denoted as V_p

I_D is at saturation or maximum, and is referred to as I_{DSS}.



JFET Operating Characteristics

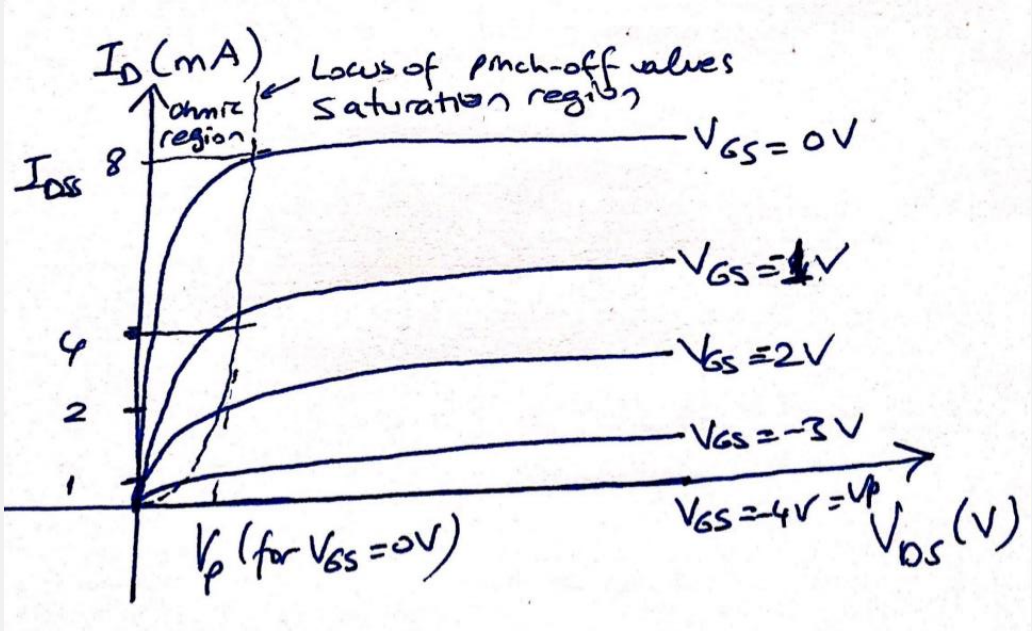
As V_{GS} becomes more negative, the depletion region increases.



JFET Operating Characteristics

As V_{GS} becomes more negative:

- The JFET experiences pinch-off at a lower voltage (V_P).
- I_D decreases ($I_D < I_{DSS}$) even when V_{DS} increases
- I_D eventually drops to 0 A. The value of V_{GS} that causes this to occur is designated $V_{GS(off)}$.

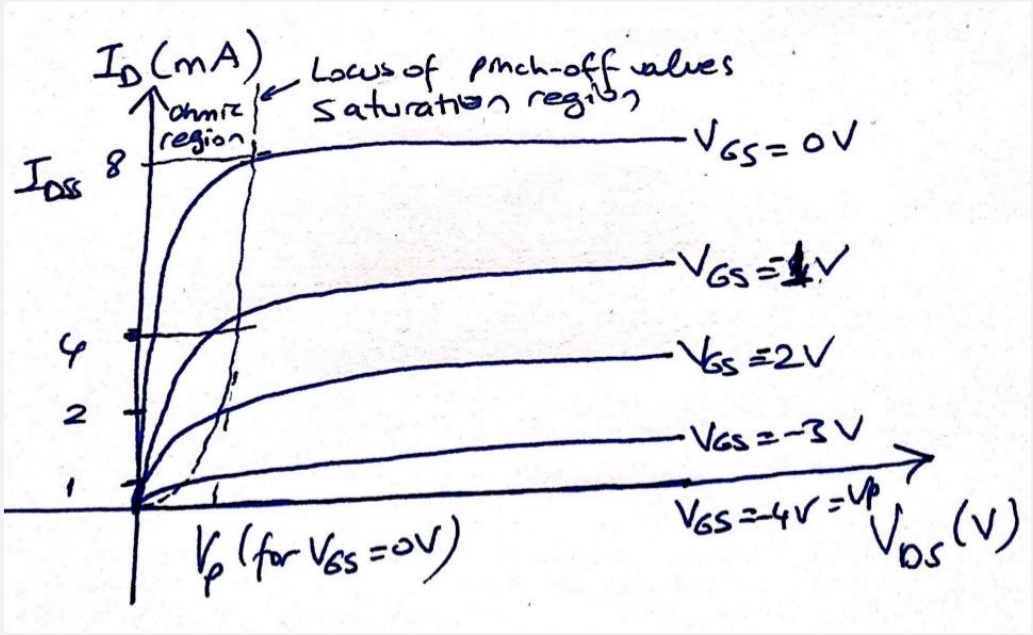


Note that at high levels of V_{DS} the JFET reaches a breakdown situation. I_D increases uncontrollably if $V_{DS} > V_{DSmax}$, and the JFET is likely destroyed.

Voltage-Controlled Resistor

The region to the left of the pinch-off point is called the ohmic region.

The JFET can be used as a variable resistor, where V_{GS} controls the drain-source resistance (r_d).

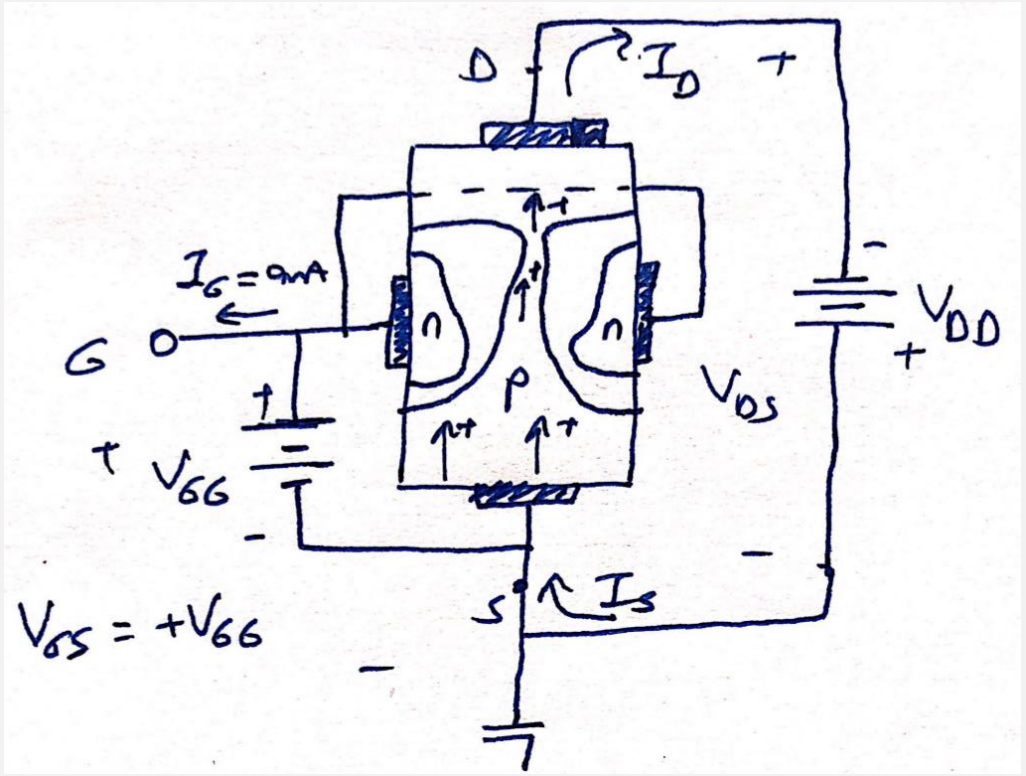


$$r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

As V_{GS} becomes more *negative*, the resistance (r_d) *increases*.

P-Channel JFETs

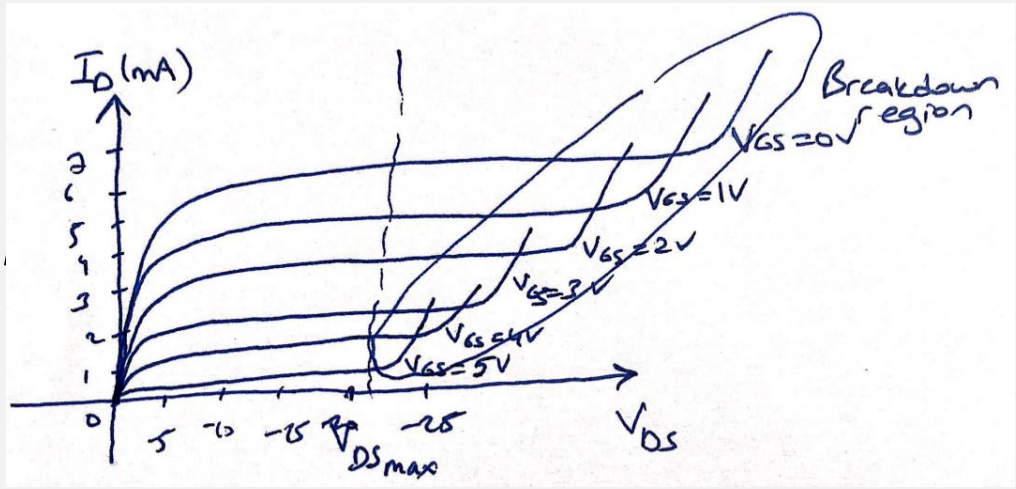
The *p*-channel JFET behaves the same as the *n*-channel JFET. The only differences are that the voltage polarities and current directions are reversed.



P-Channel JFET Characteristics

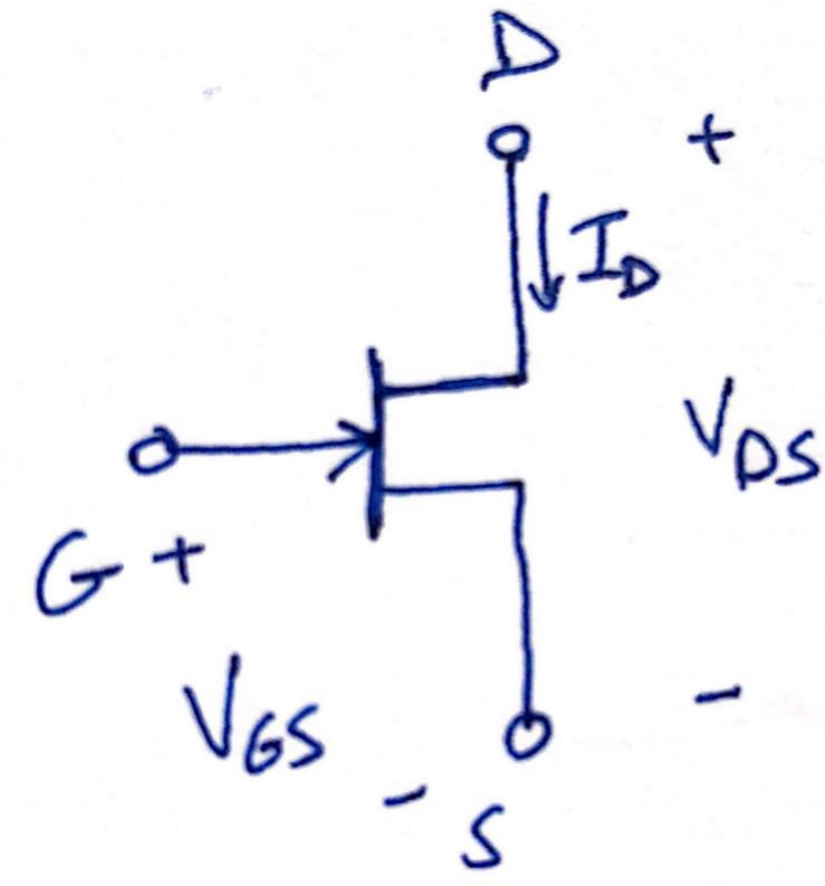
As V_{GS} becomes more positive:

- The JFET experiences pinch-off at a lower voltage (V_P).
- The depletion region increases, and I_D decreases ($< I_{DSS}$)
- I_D eventually drops to 0 A (when $V_{GS} = V_{GSoff}$)



Also note that at high levels of V_{DS} the JFET reaches a breakdown situation: I_D increases uncontrollably if $V_{DS} > V_{DSmax}$.

N-Channel JFET Symbol



JFET Transfer Characteristics

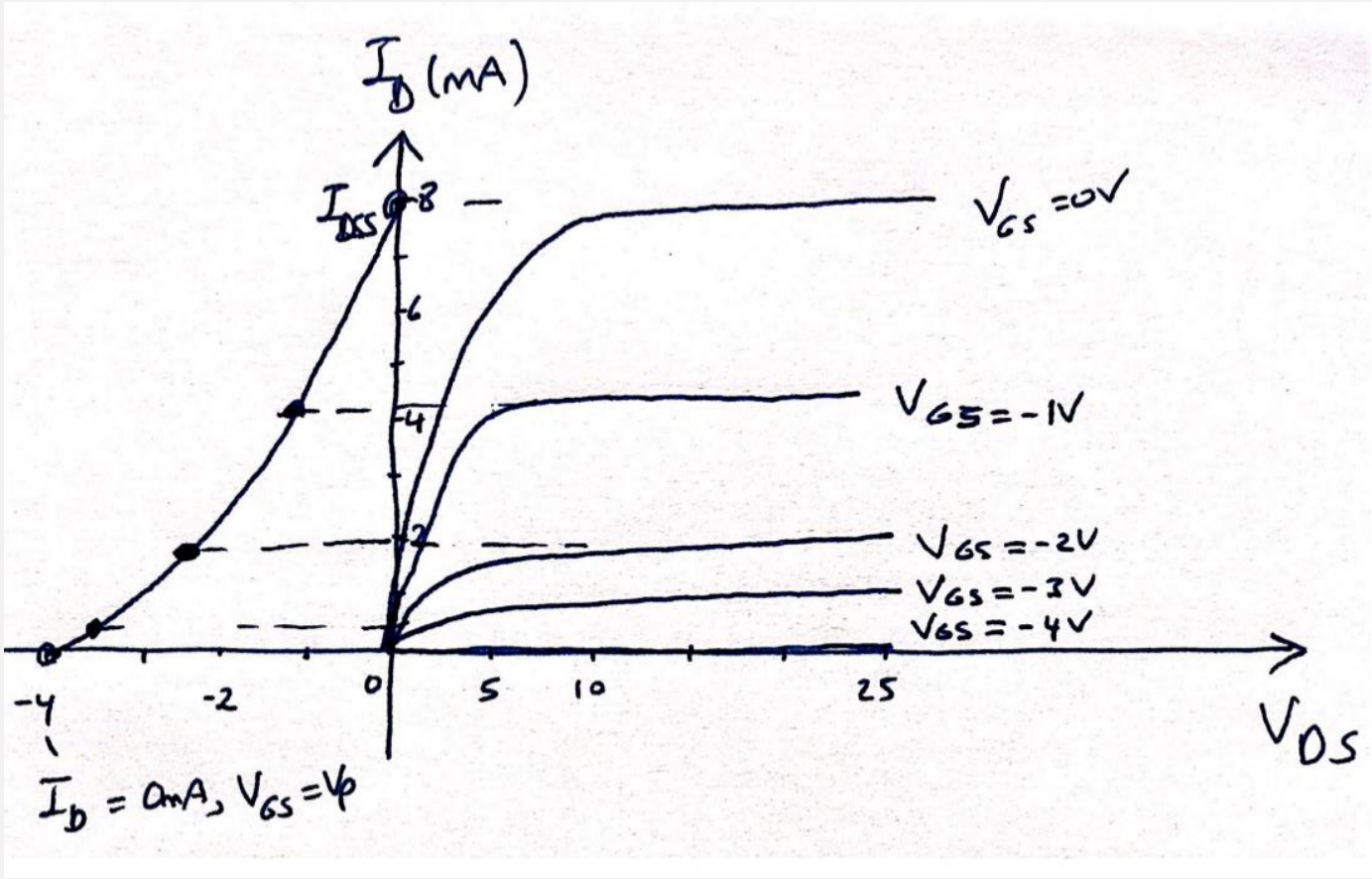
JFET input-to-output transfer characteristics are not as straightforward as they are for a BJT.

- BJT: β indicates the relationship between I_B (input) and I_C (output).

- JFET: The relationship of V_{GS} (input) and I_D (output) is a little more complicated:

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

JFET Transfer Curve



This graph shows the value of I_D for a given value of V_{GS}.

Plotting the JFET Transfer Curve

Using I_{DSS} and V_p ($V_{GS(off)}$) values found in a specification sheet, the transfer curve can be plotted according to these three steps:

1. Solving for V_{GS} = 0 V: $I_D = I_{DSS}$

2. Solving for $V_{GS} = V_{GS(off)}$: I_D = 0 A

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

3. Solving for V_{GS} = 0 V to $V_{GS(off)}$: 0 A $< I_D < I_{DSS}$

JFET Specification Sheet

Electrical Characteristics

ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	$I_G = 10\ \mu A$, $V_{DS} = 0$		–25			V
I_{GSS}	Gate Reverse Current	$V_{GS} = -15$ V, $V_{DS} = 0$ $V_{GS} = -15$ V, $V_{DS} = 0$, $T_A = 100°C$				–1.0 –200	nA nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 15$ V, $I_D = 10$ nA	5457	–0.5		–6.0	V
V_{GS}	Gate-Source Voltage	$V_{DS} = 15$ V, $I_D = 100\ \mu A$	5457		–2.5		V
ON CHARACTERISTICS							
I_{DSS}	Zero-Gate Voltage Drain Current	$V_{DS} = 15$ V, $V_{GS} = 0$	5457	1.0	3.0	5.0	mA
SMALL SIGNAL CHARACTERISTICS							
g_{fs}	Forward Transfer Conductance	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 kHz	5457	1000		5000	μmhos
g_{os}	Output Conductance	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 MHz			10	50	μmhos
C_{iss}	Input Capacitance	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 MHz			4.5	7.0	pF
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 MHz			1.5	3.0	pF
NF	Noise Figure	$V_{DS} = 15$ V, $V_{GS} = 0$, f = 1.0 kHz, $R_G = 1.0$ megohm, BW = 1.0 Hz				3.0	dB

JFET Specification Sheet

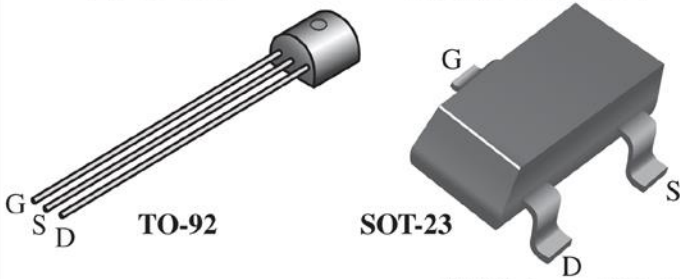
Maximum Ratings

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Units
V_{DS}	Drain-Source Voltage	25	V
V_{DG}	Drain-Gate Voltage	25	V
V_{GS}	Gate-Source Voltage	–25	V
I_{GF}	Forward Gate Current	10	mA
T_j, T_{stg}	Operating and Storage Junction Temperature Range	–55 to +150	°C

FAIRCHILD
SEMICONDUCTOR ™

2N5457 **MMBF5457**



NOTE: Source & Drain are interchangeable

N-Channel General Purpose Amplifier

This device is a low-level audio amplifier and switching transistor, and can be used for analog switching applications.

Testing JFETs

Curve Tracer

A curve tracer displays the I_D versus V_{DS} graph for various levels of V_{GS}.

Specialized FET Testers

These testers show I_{DSS} for the JFET under test.

MOSFETs

MOSFETs have characteristics similar to those of JFETs and additional characteristics that make then very useful.

There are two types of MOSFETs:

Depletion-Type

Enhancement-Type

Depletion-Type MOSFET Construction

The Drain (D) and Source (S) connect to the to *n*-type regions. These *n*-typed regions are connected via an *n*-channel. This *n*-channel is connected to the Gate (G) via a thin insulating layer of silicon dioxide (SiO_2).

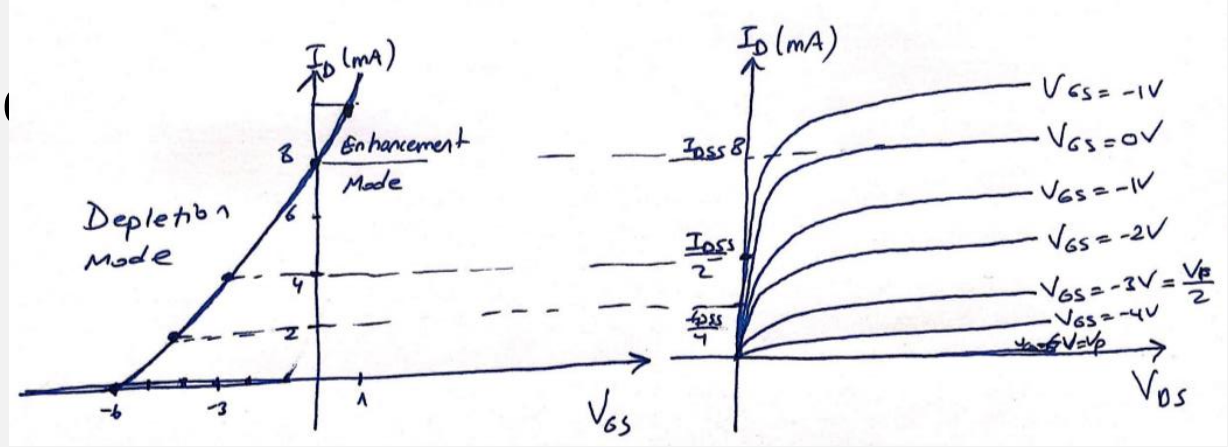
The *n*-type material lies on a *p*-type substrate that may have an additional terminal connection called the Substrate (SS).

Basic MOSFET Operation

A depletion-type MOSFET can operate in two modes:

Depletion mode

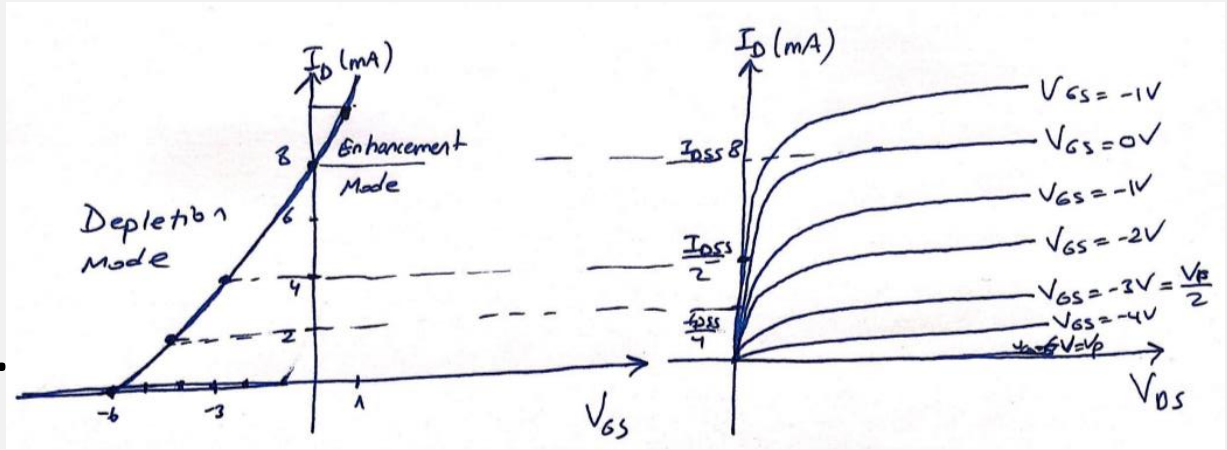
Enhancement mo



Depletion Mode Operation

(D-MOSFET)

The characteristics are similar to a JFET.



when $V_{GS} = 0$ V, $I_D = I_{DSS}$

when $V_{GS} < 0$ V, $I_D < I_{DSS}$

The formula used to plot the transfer curve for a JFET applies to a D-MOSFET as well:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

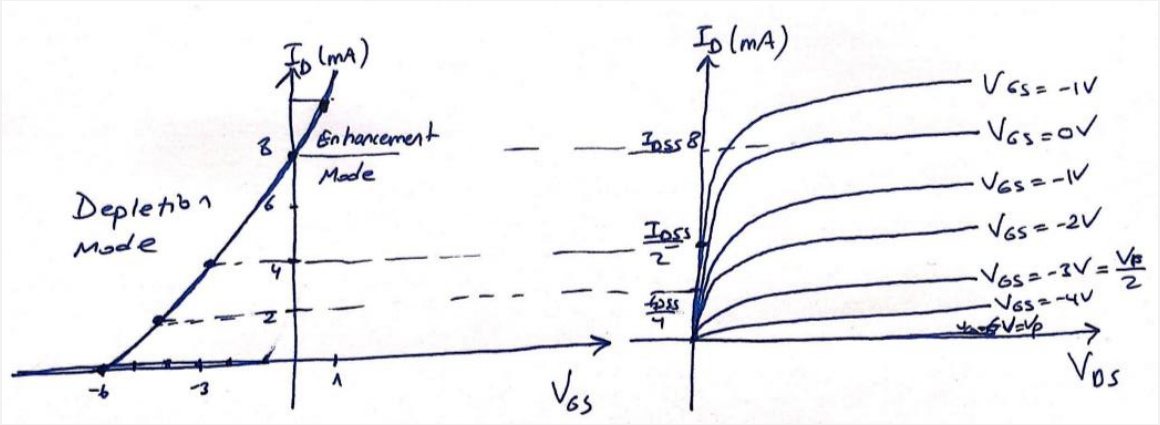
Enhancement Mode Operation

(D-MOSFET)

$V_{GS} > 0$ V, I_D increases above I_{DSS} ($I_D > I_{DSS}$)

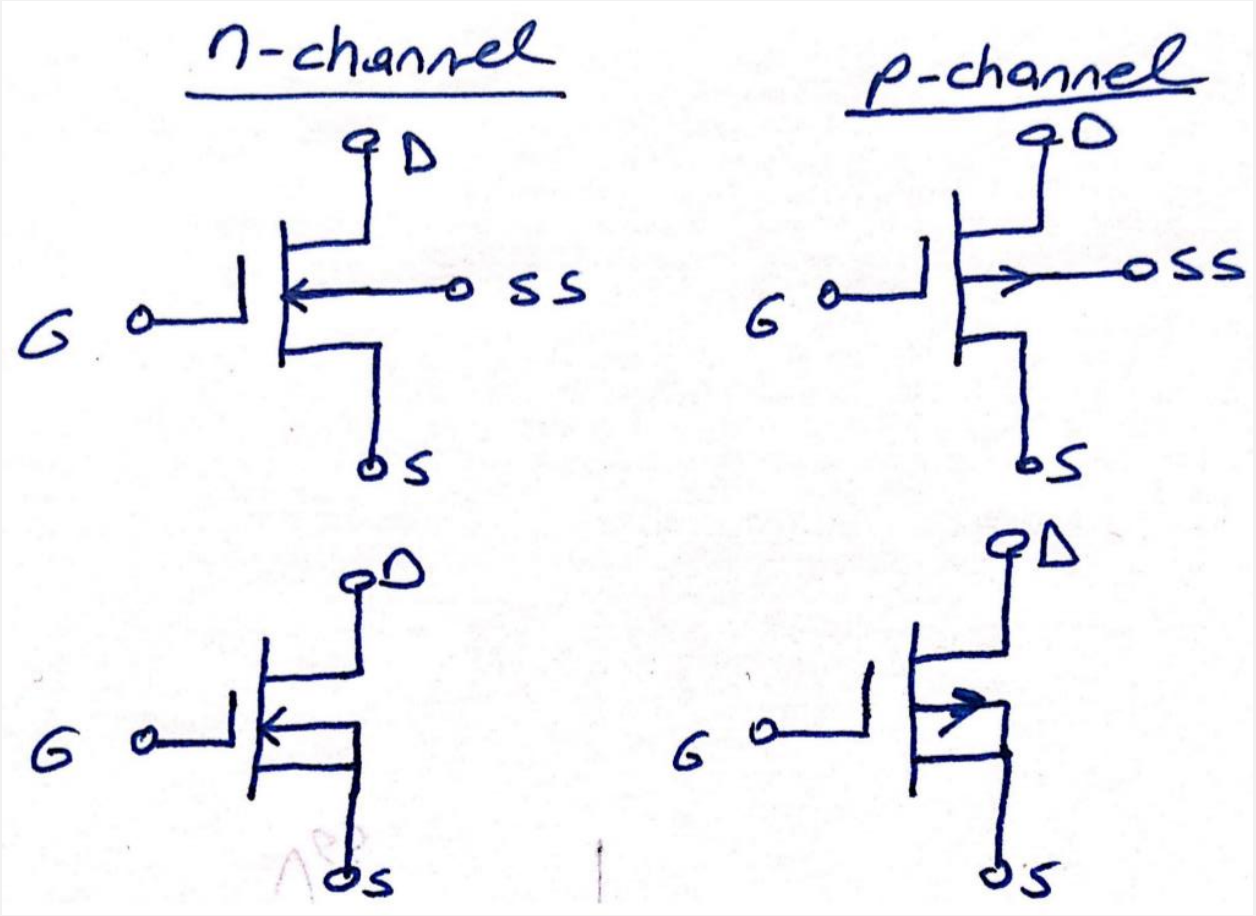
The formula used to plot the transfer curve still applies:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$



Note that V_{GS} is now positive

D-Type MOSFET Symbols



Specification Sheet

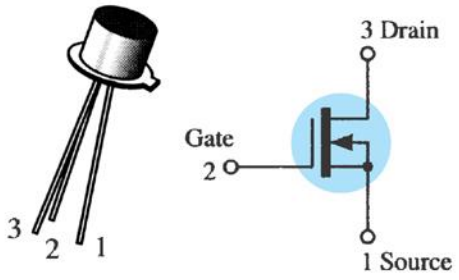
Maximum Ratings

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage 2N3797	V_{DS}	20	Vdc
Gate–Source Voltage	V_{GS}	±10	Vdc
Drain Current	I_D	20	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	200 1.14	mW mW/°C
Junction Temperature Range	T_J	+175	°C
Storage Channel Temperature Range	T_{stg}	–65 to +200	°C

2N3797

MOSFET
LOW–POWER AUDIO



N-CHANNEL – DEPLETION

Specification Sheet

Electrical Characteristics

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain Source Breakdown Voltage (V_{GS} = –7.0 V, I_D = 5.0 μA)	2N3797	$V_{(BR)DSX}$	20	25	–	Vdc
Gate Reverse Current (1) (V_{GS} = –10 V, V_{DS} = 0)		I_{GSS}	–	–	1.0	pAdc
(V_{GS} = –10 V, V_{DS} = 0, T_A = 150°C)			–	–	200	
Gate Source Cutoff Voltage (I_D = 2.0 μA, V_{DS} = 10 V)	2N3797	$V_{GS(off)}$	–	–5.0	–7.0	Vdc
Drain-Gate Reverse Current (1) (V_{DG} = 10 V, I_S = 0)		I_{DGO}	–	–	1.0	pAdc
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current (V_{DS} = 10 V, V_{GS} = 0)	2N3797	I_{DSS}	2.0	2.9	6.0	mAdc
On-State Drain Current (V_{DS} = 10 V, V_{GS} = +3.5 V)	2N3797	$I_{D(on)}$	9.0	14	18	mAdc
SMALL-SIGNAL CHARACTERISTICS						
Forward Transfer Admittance (V_{DS} = 10 V, V_{GS} = 0, f = 1.0 kHz)	2N3797	$\|y_{fs}\|$	1500	2300	3000	μmhos
(V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz)	2N3797		1500	–	–	
Output Admittance (I_{DS} = 10 V, V_{GS} = 0, f = 1.0 kHz)	2N3797	$\|y_{os}\|$	–	27	60	μmhos
Input Capacitance (V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz)	2N3797	C_{iss}	–	6.0	8.0	pF
Reverse Transfer Capacitance (V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	–	0.5	0.8	pF
FUNCTIONAL CHARACTERISTICS						
Noise Figure (V_{DS} = 10 V, V_{GS} = 0, f = 1.0 kHz, R_S = 3 megohms)		NF	–	3.8	–	dB

(1) This value of current includes both the FET leakage current as well as the leakage current associated with the test socket and fixture when measured under best attainable conditions.

E-Type MOSFET Construction

The Drain (D) and Source (S) connect to the to *n*-type regions.
These *n*-type regions are connected via an *n*-channel

The Gate (G) connects to the *p*-type substrate
via a thin insulating layer of silicon dioxide (SiO_2)

There is no channel

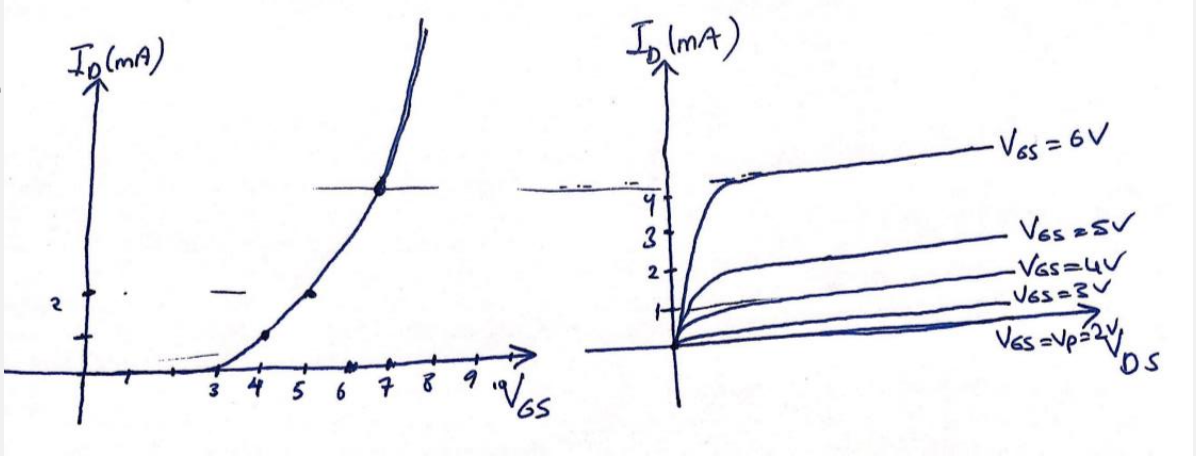
The *n*-type material lies on a *p*-type substrate
that may have an additional terminal connection
called the Substrate (SS)

E-Type MOSFET Operation

The enhancement-type MOSFET (E-MOSFET) operates only in the enhancement mode.

V_{GS} is always positive

As V_{GS} increases, I_D increases



As V_{GS} is kept constant and V_{DS} is increased, then I_D saturates (I_{DSS}) and the saturation level (V_{DSsat}) is reached

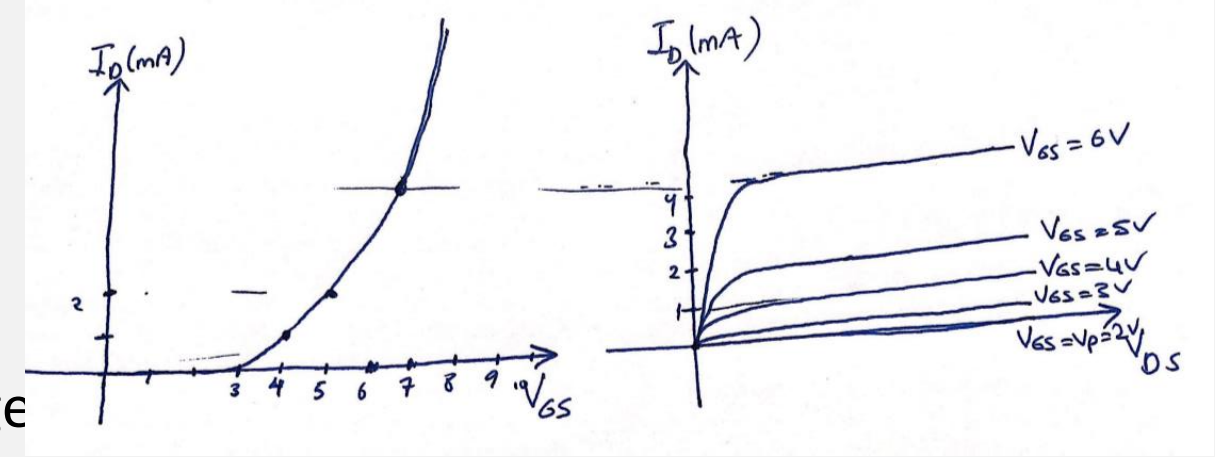
E-Type MOSFET Transfer Curve

To determine I_D given V_{GS}:

$$I_D = k(V_{GS} - V_T)^2$$

where:

V_T = the E-MOSFET threshold voltage



k, a constant, can be determined by using values at a specific point and the formula:

$$k = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2}$$

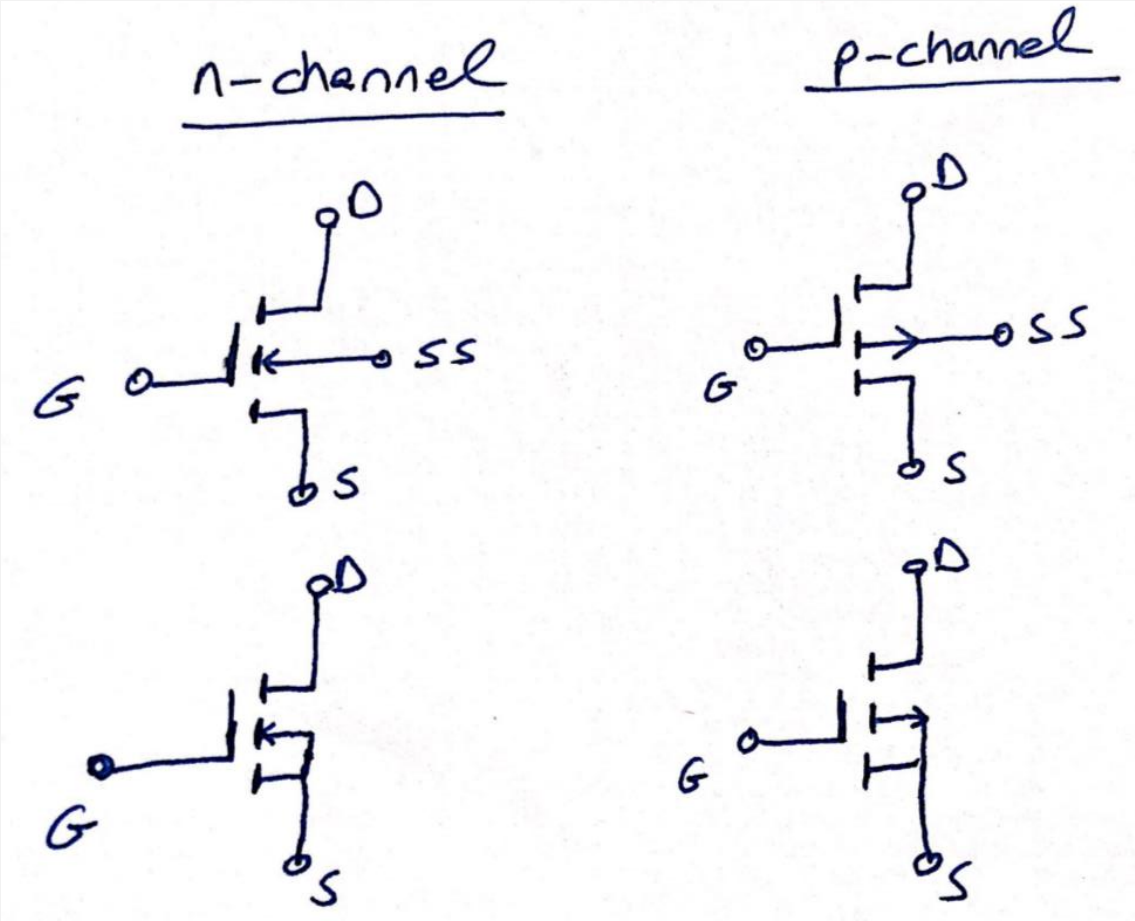
V_{DSsat} can be calculated using:

$$V_{DSsat} = V_{GS} - V_T$$

p-Channel E-Type MOSFETs

The *p*-channel enhancement-type MOSFET is similar to its *n*-channel counterpart, except that the voltage polarities and current directions are reversed.

MOSFET Symbols



Specification Sheet

Maximum Ratings

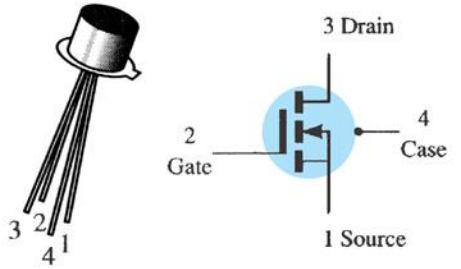
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	25	Vdc
Drain–Gate Voltage	V_{DG}	30	Vdc
Gate–Source Voltage*	V_{GS}	30	Vdc
Drain Current	I_D	30	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	300 1.7	mW mW/°C
Junction Temperature Range	T_J	175	°C
Storage Temperature Range	T_{stg}	–65 to +175	°C

* Transient potentials of ± 75 Volt will not cause gate-oxide failure.

2N4351

MOSFET
SWITCHING



N-CHANNEL – ENHANCEMENT

more…

Specification Sheet

Electrical Characteristics

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (I_D = 10 μA, V_{GS} = 0)	$V_{(BR)DSX}$	25	–	Vdc
Zero-Gate-Voltage Drain Current (V_{DS} = 10 V, V_{GS} = 0) T_A = 25°C T_A = 150°C	I_{DSS}	– –	10 10	nAdc μAdc
Gate Reverse Current (V_{GS} = ± 15 Vdc, V_{DS} = 0)	I_{GSS}	–	± 10	pAdc
ON CHARACTERISTICS				
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 10 μA)	$V_{GS(Th)}$	1.0	5	Vdc
Drain-Source On-Voltage (I_D = 2.0 mA, V_{GS} = 10V)	$V_{DS(on)}$	–	1.0	V
On-State Drain Current (V_{GS} = 10 V, V_{DS} = 10 V)	$I_{D(on)}$	3.0	–	mAdc
SMALL-SIGNAL CHARACTERISTICS				
Forward Transfer Admittance (V_{DS} = 10 V, I_D = 2.0 mA, f = 1.0 kHz)	$\|y_{fs}\|$	1000	–	μmho
Input Capacitance (V_{DS} = 10 V, V_{GS} = 0, f = 140 kHz)	C_{iss}	–	5.0	pF
Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = 0, f = 140 kHz)	C_{rss}	–	1.3	pF
Drain-Substrate Capacitance ($V_{D(SUB)}$ = 10 V, f = 140 kHz)	$C_{d(sub)}$	–	5.0	pF
Drain-Source Resistance (V_{GS} = 10 V, I_D = 0, f = 1.0 kHz)	$r_{ds(on)}$	–	300	ohms
SWITCHING CHARACTERISTICS				
Turn-On Delay (Fig. 5)	t_{d1}	–	45	ns
Rise Time (Fig. 6)	t_r	–	65	ns
Turn-Off Delay (Fig. 7)	t_{d2}	–	60	ns
Fall Time (Fig. 8)	t_f	–	100	ns

(I_D = 2.0 mAdc, V_{DS} = 10 Vdc, (V_{GS} = 10 Vdc) (See Figure 9; Times Circuit Determined))

Handling MOSFETs

MOSFETs are very sensitive to static electricity.

Because of the very thin SiO_2 layer between the external terminals and the layers of the device, any small electrical discharge can create an unwanted conduction.

Protection

- Always transport in a static sensitive bag
- Always wear a static strap when handling MOSFETS
- Apply voltage limiting devices between the gate and source, such as back-to-back Zeners to limit any transient voltage.

VMOS Devices

VMOS (vertical MOSFET) is a component structure that provides greater surface area.

Advantages

VMOS devices handle higher currents by providing more surface area to dissipate the heat.

VMOS devices also have faster switching times.

CMOS Devices

CMOS (complementary MOSFET) uses a p-channel and n-channel MOSFET; often on the same substrate as shown here.

Advantages

- Useful in logic circuit designs
- Higher input impedance
- Faster switching speeds
- Lower operating power levels