BME 212 Electronics Laboratory

Experiment #5 BJT Amplifiers – Small Signal Analysis

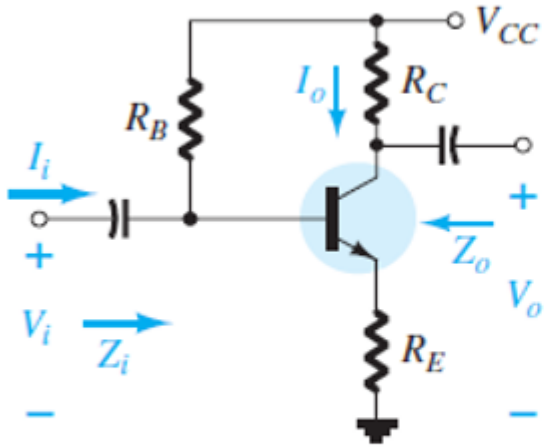
Objective

The objective of this experiment is to study the AC levels for the variety of important BJT biasing configurations and understanding the effect of transistor parameters on small signal analysis.

Preliminary Work

1- For given circuits below using given biasing conditions calculate the I_B, I_E, V_{CEQ}, r_e, Z_{in}, Z_{out}, A_v and plot the output voltage corresponding the sinusoidal input voltage (V_{CC} = 12 V, V_i = 2 V_{pp} (for a and c), β = 150, coupling capacitor values are 10 uF, F = 1 kHz).

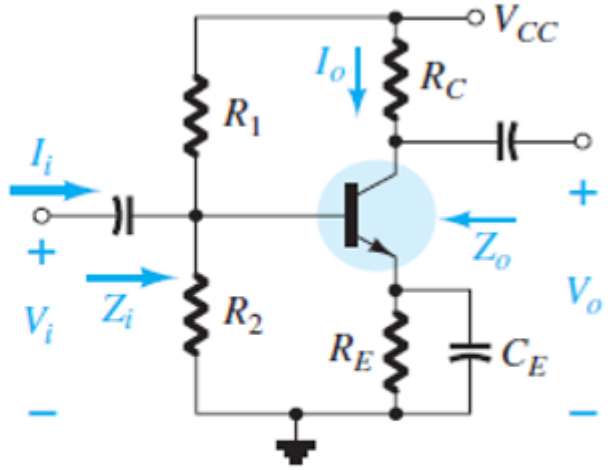
a)



(Emitter bias configuration)

(R_B = 560 kΩ , R_C = 2.2 kΩ, R_E = 750 Ω)

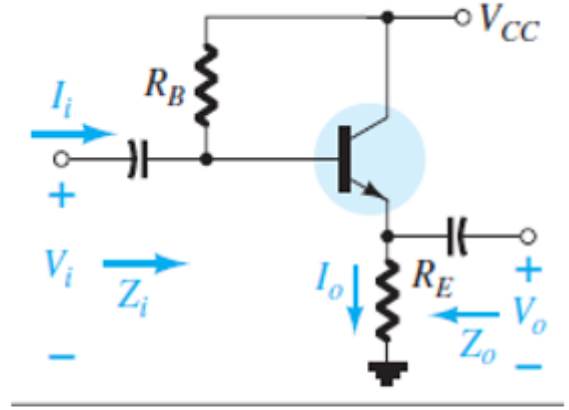
b)



(Voltage-divider bias configuration)

(R_1 = 33 kΩ, R_2 = 10 kΩ, R_C = 750 Ω, R_E = 1.5 k Ω, V_i = 100 mV_{pp})

c)

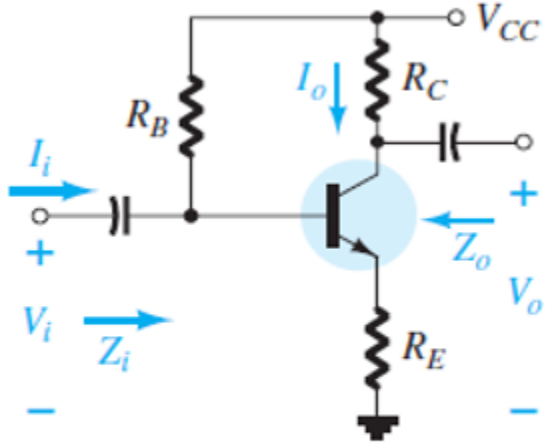


(Emitter follower configuration)

(R_B = 220 kΩ , R_E = 3.3 kΩ)

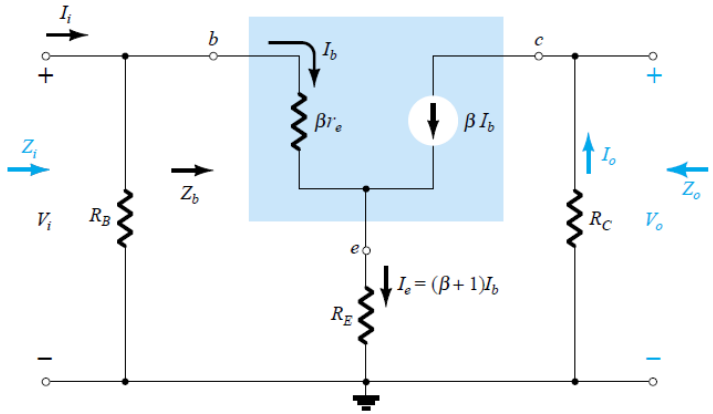
Preliminary Work (Cont.)

a)



(Emitter bias configuration)

(R_B = 560 kΩ , R_C = 2.2 kΩ, R_E = 750 Ω)



Hints:

DC: $I_B = \dfrac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$

$I_E = (\beta + 1)I_B$

$r_e = \dfrac{26\ \text{mV}}{I_E}$

$V_{CE} = V_{CC} - I_C(R_C + R_E)$

$Z_b = \beta r_e + (\beta + 1)R_E$

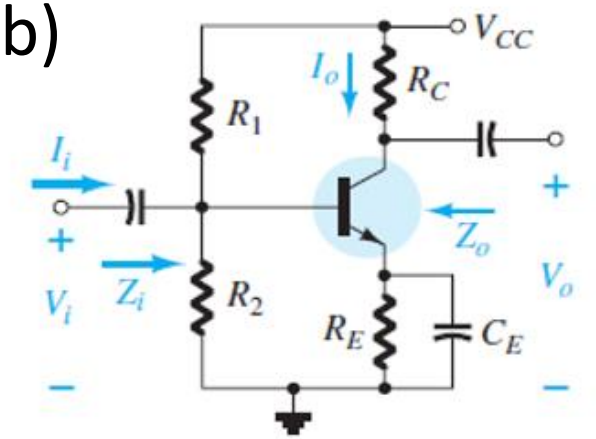
$Z_i = R_B \| Z_b$

$Z_o = R_C$

$A_v = \dfrac{V_o}{V_i} = -\dfrac{\beta R_C}{Z_b}$

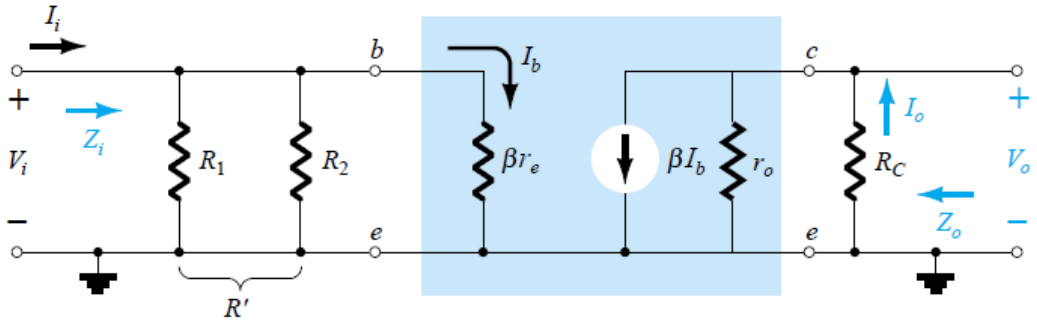
Preliminary Work (Cont.)

b)



(Voltage-divider bias configuration)

(R_1 = 33 kΩ, R_2 = 10 kΩ, R_C = 750 Ω, R_E = 1.5 k Ω, V_i = 100 mV_{pp})



Hints:

DC: Testing $\beta R_E > 10R_2$

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$V_E = V_B - V_{BE}$$

$$I_E = \frac{V_E}{R_E}$$

$$r_e = \frac{26\ \text{mV}}{I_E}$$

$$R' = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

$$Z_i = R' \| \beta r_e$$

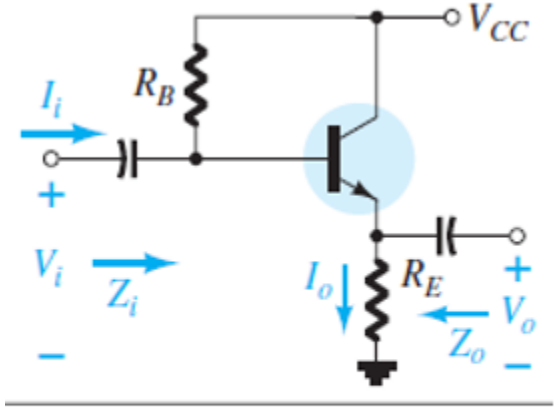
$$Z_o = R_C \| r_o$$

$$Z_o \cong R_C \qquad r_o \geq 10R_C$$

$$A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{r_e} \qquad r_o \geq 10R_C$$

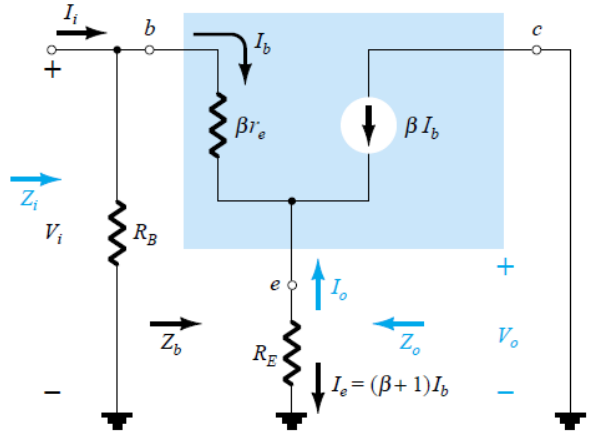
Preliminary Work (Cont.)

c)



(Emitter follower configuration)

($R_B = 220\ k\Omega$, $R_E = 3.3\ k\Omega$)



Hints:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$I_E = (\beta + 1)I_B$$

$$r_e = \frac{26\ \text{mV}}{I_E}$$

$$Z_i = R_B \| Z_b$$

$$Z_b = \beta r_e + (\beta + 1)R_E$$

$$I_e \cong \frac{V_i}{r_e + R_E}$$

$$Z_o = R_E \| r_e$$

$$A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e}$$

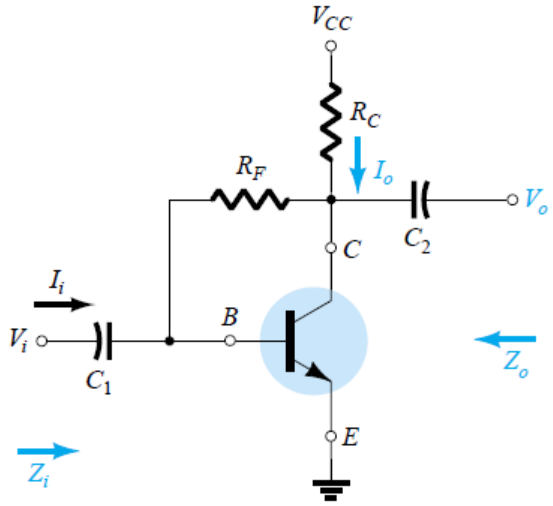
Since R_E is usually much greater than r_e,

$$A_v = \frac{V_o}{V_i} \cong 1$$

Preliminary Work (Cont.)

2- Design a collector feedback bias circuit by calculating resistor values for a npn transistor to achive given conditions: $A_v = -169$, $Z_i = 692\ \Omega$, $Z_o = 995.4\ k\Omega$, $V_{CC} = 9\ V$, $\beta = 250$ and $I_E = 4.4\ mA$. To implement the circuit, design it using close nominal resistor values from the component list given as: 750 Ω, 1 k Ω, 3.3 k Ω, 50 kΩ, 150 k Ω, 220 kΩ

(**Note**: Use approximated solutions in your calculations)



Procedure

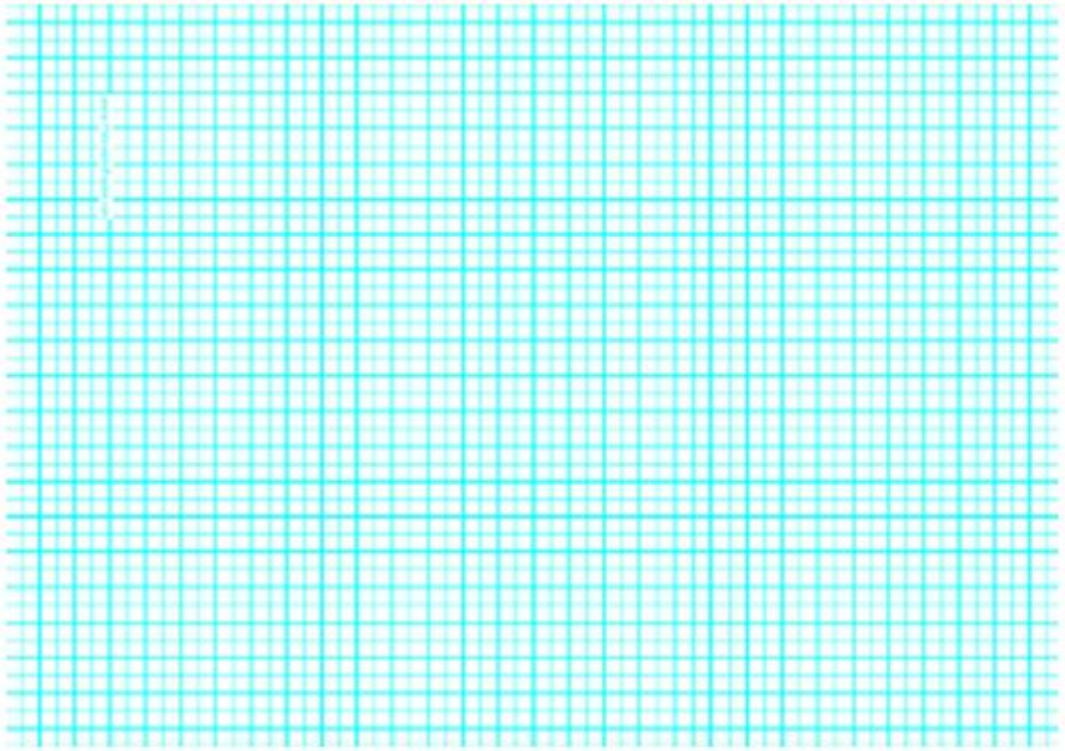
CHECK ALL THE TRANSISTORS USING MULTIMETER BEFORE START.

1) For given circuits in Preliminary Work 1, measure the I_E and V_{CEQ}, plot the output voltages, calculate the voltage gain A_v and compare the results with Preliminary Work 1.

2) Set up your circuit designed in Preliminary Work 2. For 10 mV_{pp} sinusoidal input voltage plot the output voltage of the circuit, calculate the A_v and compare with Preliminary Work 2.

BME212 Report#5 Results

1) Plot output voltage and obtain I_E, V_{CEQ}, A_v



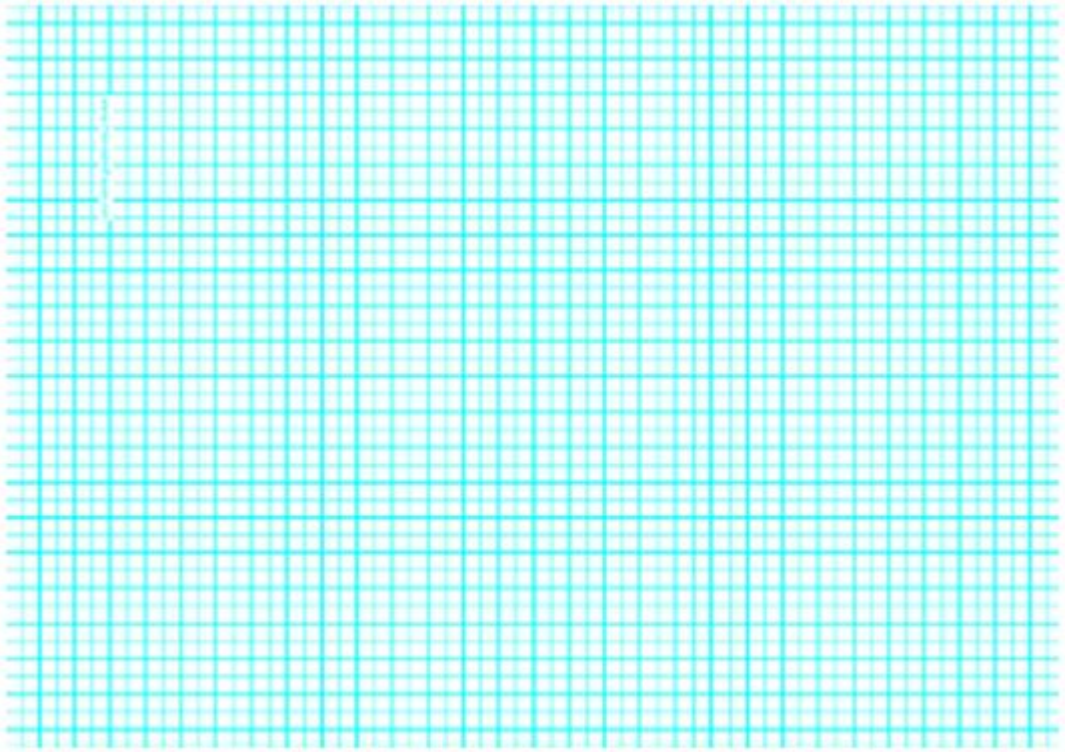
(Emitter bias configuration)

	I_E	V_{CEQ}	A_V
Measured			
Calculated			

Comment :

BME212 Report#5
Results (Cont.)

1) Plot output voltage and obtain I_E, V_{CEQ}, A_V



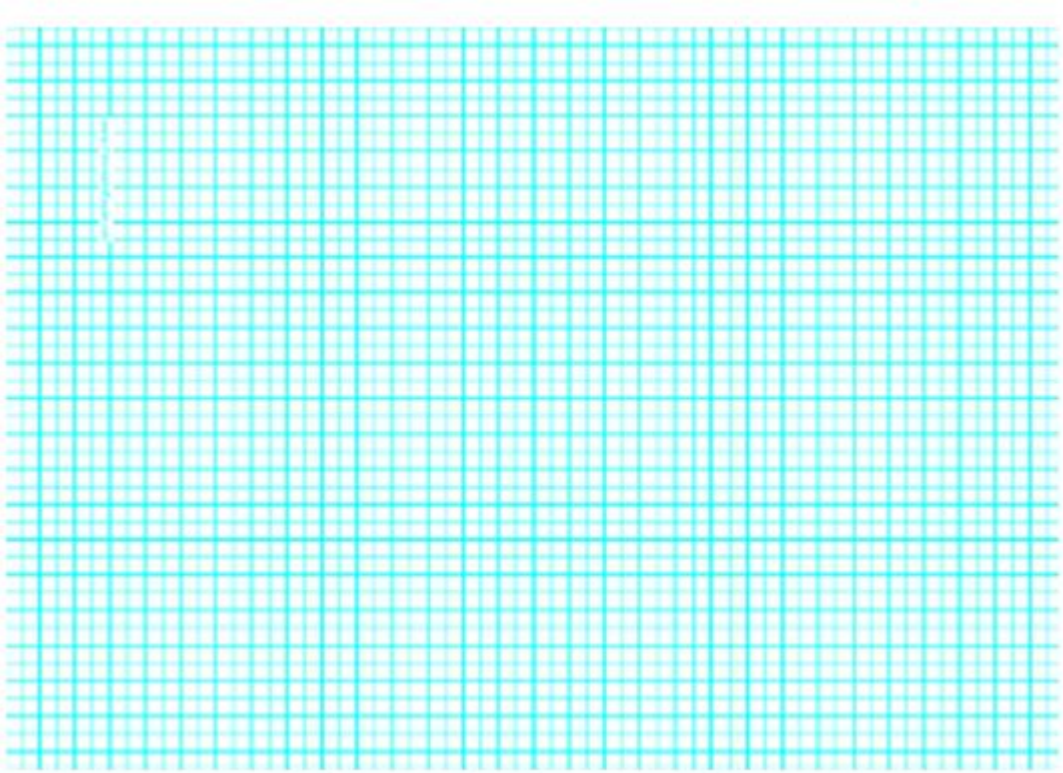
(Voltage-divider bias configuration)

	I_E	V_{CEQ}	A_V
Measured			
Calculated			

Comment :

BME212 Report#5
Results (Cont.)

1) Plot output voltage and obtain I_E, V_{CEQ}, A_V



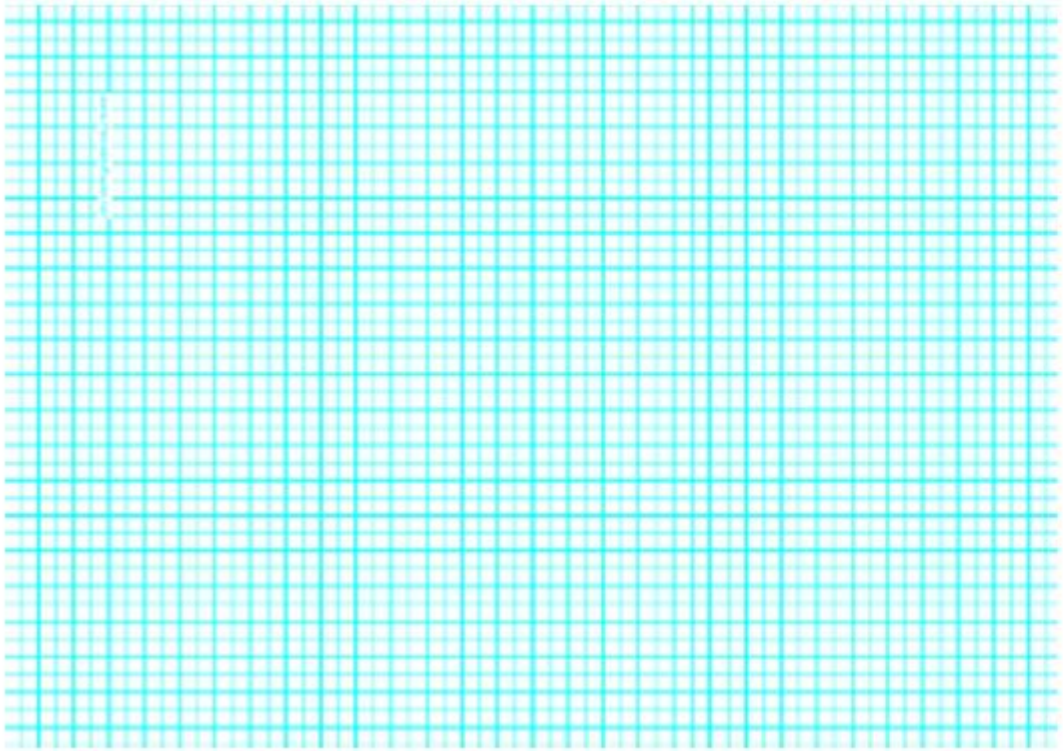
(Emitter follower configuration)

	I_E	V_{CEQ}	A_V
Measured			
Calculated			

Comment :

BME212 Report#5
Results (Cont.)

2) Plot output voltage and obtain A_V



(Collector feedback bias configuration)

	A_V
Measured	
Calculated	

Comment :