BME 212 Electronics Laboratory

Experiment #9 FET Amplifiers - Small Signal Analysis using Multisim

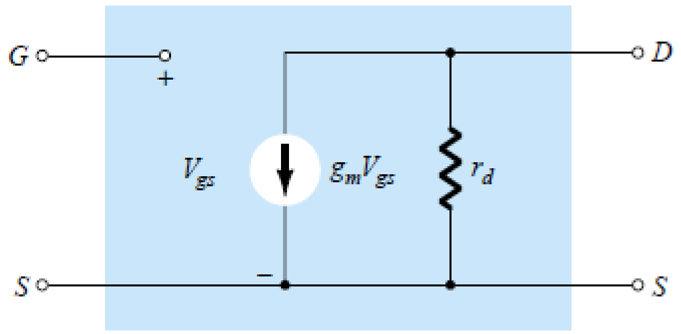
Objective

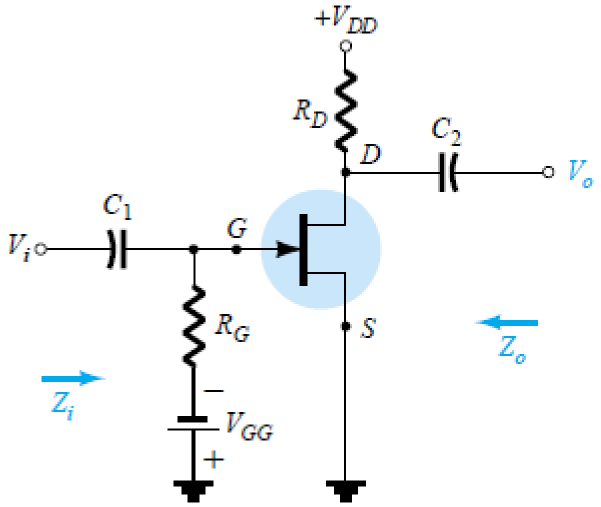
The objective of this experiment is to study the AC levels for the variety of important FET biasing configurations and understanding the effect of transistor parameters on small signal analysis.

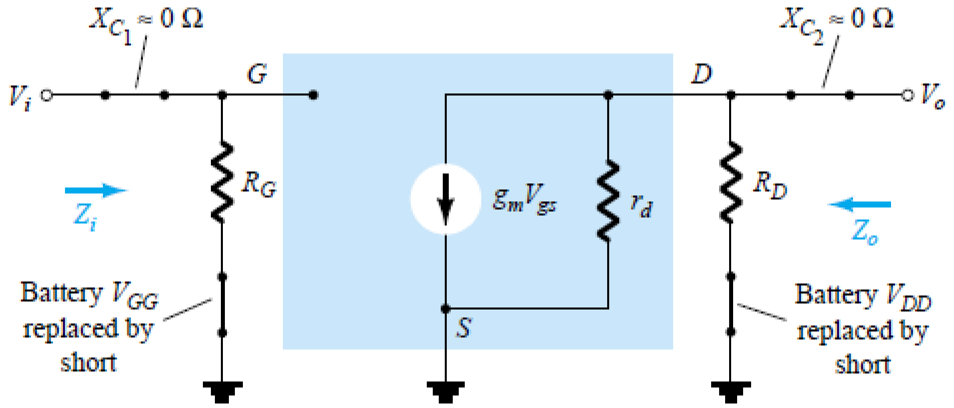
Preliminary Work

1. Study the small signal analysis of field effect transistors (FET) in Chapter 9 of the Electronic Devices and Circuit Theory book.

JFET Fixed-Bias Configuration







$$Z_i = R_G$$

$$Z_o = R_D \| r_d$$

$$Z_o \cong R_D \quad {}_{r_d \geq 10 R_D}$$

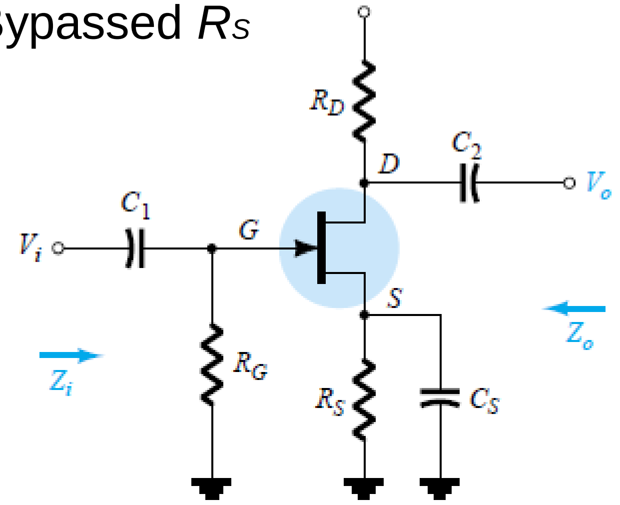
$$A_v = \frac{V_o}{V_i} = -g_m (r_d \| R_D)$$

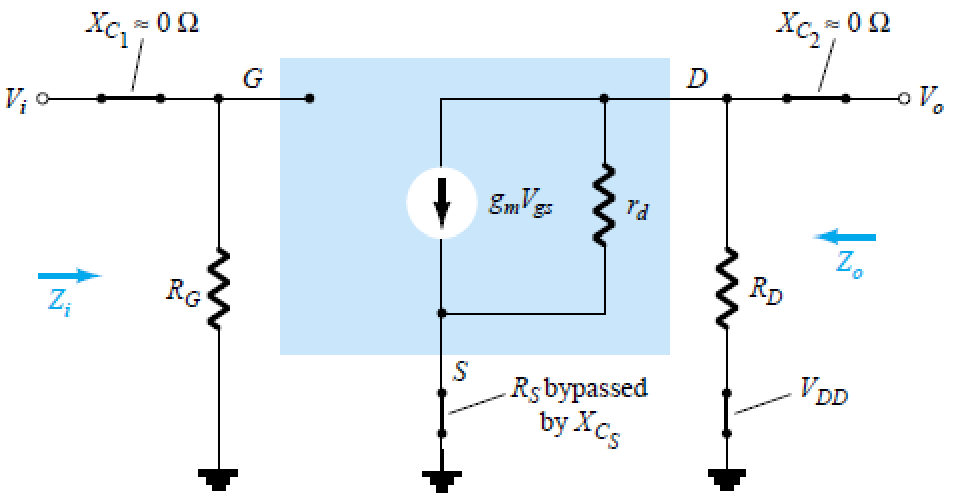
$$A_v = \frac{V_o}{V_i} = -g_m R_D \quad {}_{r_d \geq 10 R_D}$$

Preliminary Work (Cont.)

JFET Self-Bias Configuration

Bypassed R_S





$$Z_i = R_G$$

$$Z_o = R_D \| r_d$$

$$A_v = -g_m(r_d \| R_D)$$

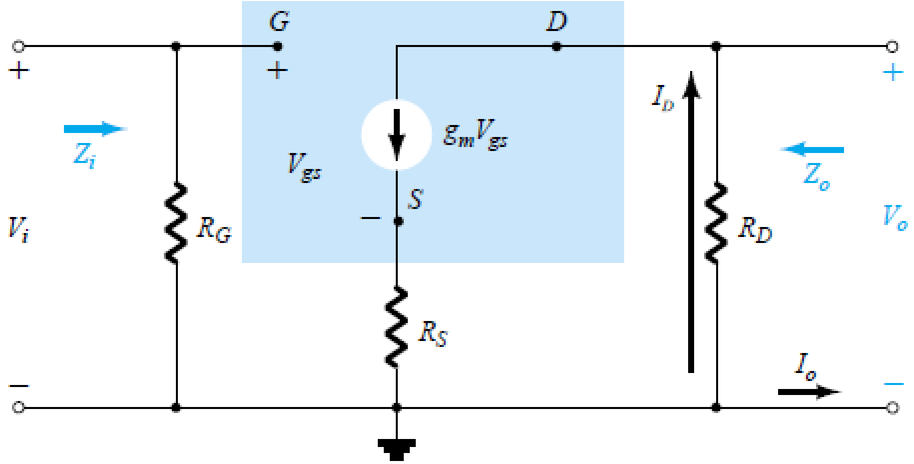
$$Z_o \cong R_D \quad {}_{r_d \geq 10R_D}$$

$$A_v = -g_m R_D \quad {}_{r_d \geq 10R_D}$$

Preliminary Work (Cont.)

JFET Self-Bias Configuration

Unbypassed *R*s



$$Z_i = R_G$$

$$Z_o = \frac{V_o}{I_o} = R_D \quad r_d = \infty\Omega$$

$$Z_o = \frac{\left[1 + g_mR_S + \frac{R_S}{r_d}\right]}{\left[1 + g_mR_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]} R_D$$

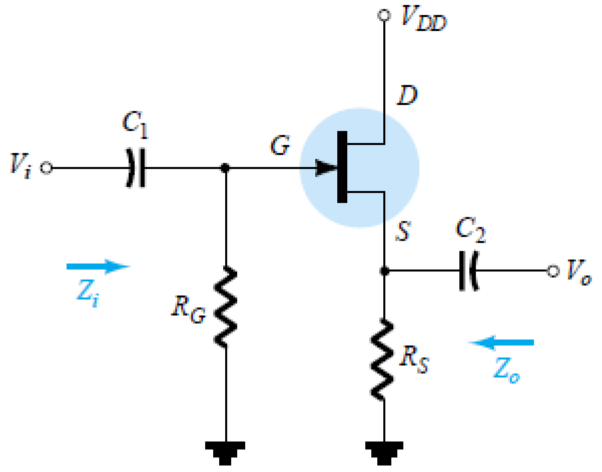
$$Z_o = R_D \quad r_d \geq 10R_D$$

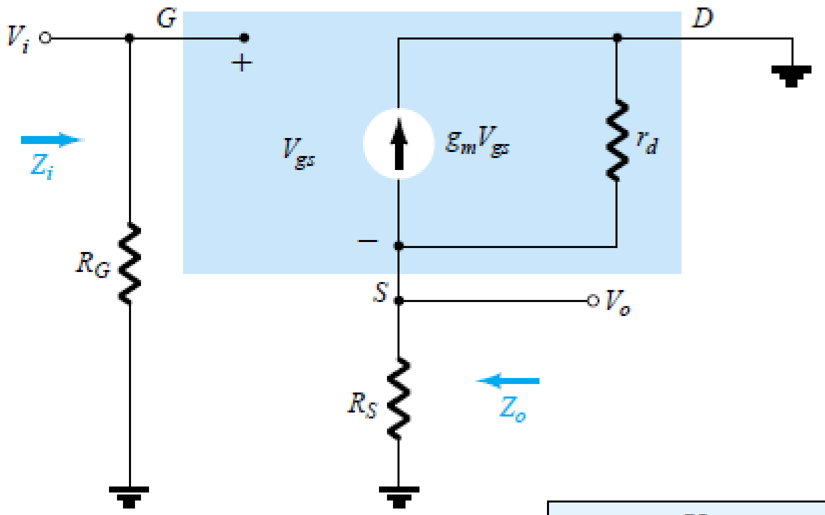
$$A_v = \frac{V_o}{V_i} = -\frac{g_mR_D}{1 + g_mR_S + \frac{R_D + R_S}{r_d}}$$

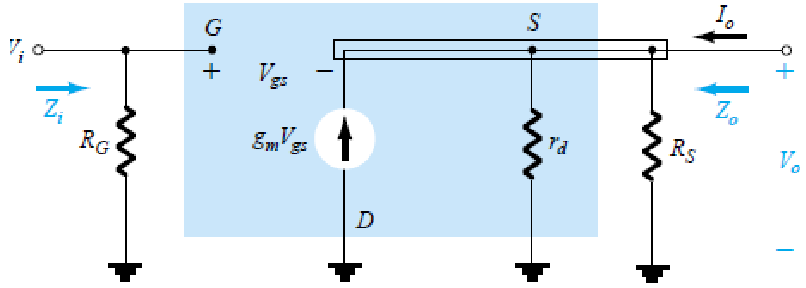
$$A_v = \frac{V_o}{V_i} = -\frac{g_mR_D}{1 + g_mR_S} \quad r_d \geq 10(R_D + R_S)$$

Preliminary Work (Cont.)

JFET Source-Follower (Common-Drain) Configuration







$$Z_i = R_G$$

$$Z_o = r_d \| R_S \| \ 1/g_m$$

$$A_v = \frac{V_o}{V_i} = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)}$$

$$Z_o \cong R_S \| 1/g_m$$ $r_d \geq 10R_S$

$$A_v = \frac{V_o}{V_i} \cong \frac{g_m R_S}{1 + g_m R_S}$$ $r_d \geq 10R_S$

Procedure

1) Set up the circuits A, B, C and D given below. For all circuits observe $v_{in}(t)$ and $v_o(t)$. Draw $v_o(t)$ into the graph paper, calculate voltage gain (Av) theoretically and practically (using input and output voltage ratio).

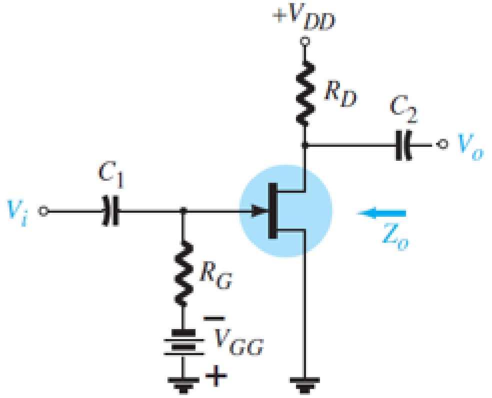
Note: For all circuits 2N3370 coded FET will be used. For this model some parameters will be ajdusted as follows:

Right click to the FET >> Properties >> Edit Model >> Thresholding Voltage = -1.5 V, Transconductance parameter = 0.01, Drain ohmic resistance = 2 kΩ >> Enter >> Change component >> Ok

For all circuits capacitors are **10μF** and g_m = **6.6 mS**.

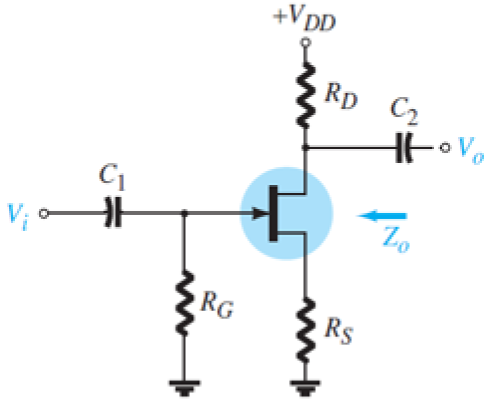
Procedure (Cont.)

A.



(V_{DD} = 20 V,RG = 2 MΩ R_D = 2 kΩ, V_{GG} = -1.2 V,
Vin = 40 mVpp / 1kHz) Av = -gm.R_D

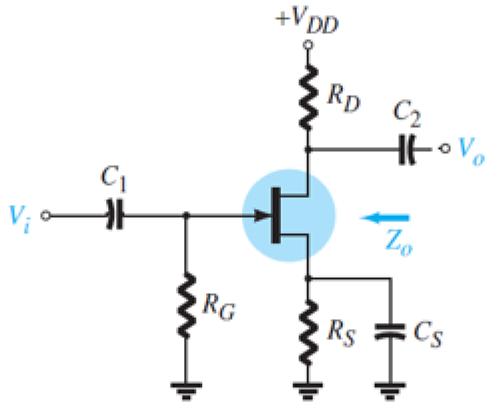
B.



(V_{DD} = 20 V, R_G = 2 MΩ R_D = 2 kΩ, R_S = 840 Ω,
Vin = 2 Vpp/1kHz) Av = (-gm.R_D / (1+ gm.Rs))

Procedure (Cont.)

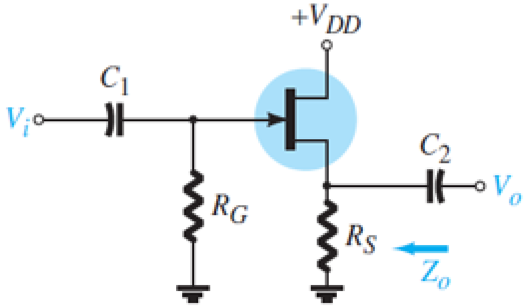
C.



(V_{DD} = 20 V, R_G = 2 MΩ R_D = 4 kΩ, R_S = 1 kΩ,

Vin = 40 mVpp/1kHz) Av = -gm.R_D

D.



(V_{DD} = 20 V, R_G = 2 MΩ, R_S = 2.2 kΩ,

Vin = 2 Vpp/1kHz) Av = (gm.R_D / (1+ gm.Rs))

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Results

1) Draw output voltages.

A.

A_v threrotical	
A_v practical	

Comment:

B.

A_v threrotical	
A_v practical	

Comment:

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Results (Cont.)

C.

A_V threrotical	
A_V practical	

Comment:

D.

A_V threrotical	
A_V practical	

Comment: